CASSINI/CAPS
CPU 1 FLIGHT SOFTWARE
FUNCTIONAL DESIGN DOCUMENT

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1 INTRODUCTION

1.1 Identification and Scope

This document is the Flight Software Functional Design (FSFD) for the Cassini Plasma Spectrometer (CAPS) flight software, document number 5548-FSFD-01. CAPS consists of an Ion Mass Spectrometer (IMS), an Electron Spectrometer (ELS), an Ion Beam Spectrometer (IBS), an Actuator (ACT), and a Data Processing Unit (DPU). The DPU consists of two (2) Central Processing Unit (CPU) boards each of which contains one 1750A microprocessor. Data from the IMS is acquired and processed by the Spectrum Analyzer Module (SAM) which also contains a 1750A microprocessor. This document presents the functional design for the CAPS Data Processing Unit (DPU) CPU 1. This document only defines the functional design for CPU 1. CPU 2 functional design is described in document 5548-FSFD-02. The SAM functional design is described in 5548-FSFD-03. The CAPS investigation is being developed by Southwest Research Institute under JPL Contract No. 958964.

Chapter 1 identifies this document, its scope, purpose, objectives, and conventions. Chapter 2 lists the applicable documents referenced by this FSFD. Chapter 3 contains a high level flight software functional specification. The specification includes a narrative description of the CPU 1 flight software modes. Chapter 4 presents an overview of the hardware functional design. This chapter contains memory maps for the hardware components of CAPS and descriptions of the hardware operation under software control. Chapter 5 is the flight software function design description. This chapter contains sections on data acquisition, telemetry generation, and command processing.

Appendix A lists the acronyms used in this document. Appendix B contains the Requirements Traceability Matrix. This matrix cross-references the CAPS requirements documented in 5548-FSRD-01, the Flight Software Requirements Document, and ensures that the applicable requirements have been addressed by this functional design. Appendix C contains the compression encoding algorithm used by CPU 1 flight software to compress 16-bit unsigned values to 8-bit unsigned values. Appendix D lists the high voltage commanding tolerance tables.. Appendix E lists the CPU 1 PROM sequences. Appendix F lists the IBS sweep and STIM tables. Appendix G lists the HVU2 sweep tables. Appendix H lists the BIU descriptor table configuration. Appendix I contains the maintenance housekeeping stream format. Appendix J contains the CAPS maintenance housekeeping stream parameter limits. Appendix K contains the CAPS science (normal) housekeeping stream format. Appendix L contains the CAPS science housekeeping stream format parameter limits. Appendix M contains the actuator wobble compensation tables. Appendix N contains the CAPS command summary and formats. Appendix I-N present information that is requested by JPL for inclusion in a number of the project's CAS-3-xxx documents. The format of the information in some of the appendices was dictated by JPL requirements/requests.

1.2 Purpose and Objectives

The purpose of this FSFD is to establish the algorithms, functions, timing, and formats CPU 1 flight software provides and uses to meet the requirements and goals set forth in 5548-FSRD-01, the Flight Software Requirements Document. The objectives of this FSFD are to:

1) Establish the design baseline from which the Flight Software Detailed Design shall be produced.
2) Provide a level of functional design detail sufficient to document resource usage, telemetry formats, commands, spacecraft interface protocols, functional timing, algorithmic specifications, mode changing, and inter-processor communications protocols.
3) Provide traceability from 5548-FSRD-01 to 5548-FSDD-01.
4) Fulfill in part the functional design software development phase as documented in the Cassini/CAPS Work Implementation Plan (WIP), 5548-WIP-01.

1.3 Maintenance and Traceability

This document is governed by the CAPS Work Implementation Plan (WIP). As described in the WIP, upon sign-off this document shall be put under document control as dictated by SwRI OP-05-15-101, Document Control. Changes to this document require approval on the Revision Record page of this document. Revisions to this document require the re-release of the cover page with approval signatures.

2 APPLICABLE DOCUMENTS

The following documents and standards form a part of this document to the extent specified in the body of this document. In cases where no date is shown for a document, the latest issue shall be assumed. In the event of a conflict between the contents of this document and the contents of one or more of the referenced documents, this document shall take precedence.

2.1 JPL Documents

PD 699-510	CRAF/Cassini Software Management Plan
JPL D-4000	JPL Software Management Standards Package, Version 3.0
JPL D-9992	CDS-Bus Interface Unit Design Package
CAS-3-271	Cassini Orbiter Functional Requirements Book Spacecraft Intercommunications
CAS-3-281	Cassini Orbiter Telemetry Formats and Measurements
CAS-3-291	Cassini Orbiter Uplink Formats and Command Tables
CAS-3-310	Cassini Oribiter Functional Requirements Book Spacecraft Information System
ECR 101094	Engineering Change Request, CDS Ver. 9.0 STMs

2.2 SwRI Documents

OP-05-15-101	Document Control
5548-IDD	CAPS Instrument Description Document
5548-FSSRD	CAPS Flight Software Science Requirements Document
5548-FSRD-01	CAPS Flight Software Requirements Document
5548-FSFD-02	CAPS Flight Software Functional Design for CPU 2
5584-FSFD-03	CAPS Flight Software Functional Design For SAM
5548-IBS	IBS Interface Control Document
5548-ELS	ELS Interface Control Document
5548-HVU-1	HVU1 Interface Control Document
5548-HVU-2	HVU2 Interface Control Document
5548-SAM	SAM Interface Control Document
5548-TDC	TDC Interface Control Document
5548-ACT	ACT Interface Control Document
15-05759-CAPSSRD-01	Cassini/CAPS Delta Software Requirements Document

3 FLIGHT SOFTWARE DESCRIPTION AND SPECIFICATIONS

3.1 Flight Software Description

3.1.1 Overview

CAPS consists of an Ion Mass Spectrometer (IMS), an Electron Spectrometer (ELS), an Ion Beam Spectrometer (IBS), an Actuator (ACT), and a Data Processing Unit (DPU) all of which are controlled and/or configured by the CAPS Flight Software (CFS) via commands from the spacecraft (S/C) Command and Data System (CDS). For an overview of the CAPS investigation at a system level, reference the Instrument Description Document (5548-IDD). The DPU consists of two (2) Central Processing Unit (CPU) boards designated CPU 1 and CPU 2. Each CPU board contains a PACE family 1750A microprocessor, a 1742 Memory Management Unit (MMU), and a 1745 Peripheral Interface Controller (PIC) from Performance Semiconductor Corporation. In addition, data from the IMS is acquired and processed by the Spectrum Analyzer Module (SAM) which contains a third 1750A processor.

CAPS will be assigned power, data rate, and memory resources on a daily basis during the mission. Data resources will be allocated by volume on the S/C Solid State Recorder (SSR). Management of the CAPS data volume will be through the choice of operating modes and data compression strategy. CAPS commands will be uplinked to the spacecraft and stored in the CAPS memory as command sequences. Triggers for executing these command sequences are stored in the CDS. The command triggers are time-tagged and are sent by the CDS to CAPS for execution at the appropriate time. Uplink is planned to take place once every 28 days. The Cassini Project's concept of Instrument Expanded Blocks (IEB) and “distributed processing” are used in implementing the CAPS command process (see CAS-3-310).

Spacecraft operational modes are described in 5548-FSSRD, the CAPS Flight Software Science Requirements Document. The operational modes define CAPS operating state, data rate, data product types (housekeeping and/or science data), and power allocation. Within the data rate assigned to CAPS by the S/C operational mode (termed the “physical data rate”) will be a number of logical data rates. The logical data rates used during a S/C operational mode will be less than or equal to the physical data rate assigned to that mode. The logical data rates will be used to manage the volume of data sent to the CDS over time. In this way the science data flow can be tailored within the allocated CAPS volume so that peak data production occurs during anticipated scientifically significant areas of an orbit.

CPU 1 flight software provides communication with the spacecraft, functions for the management of allocated resources (power, SSR memory, and telemetry bandwidth), an interface to CPU 2, and mode change functions. CPU 1 flight software monitors, controls, and acquires data from the CAPS power supplies, the ELS and IBS sensors, and the actuator.

3.1.2 CPU 1 Flight Software Objectives

CPU 1 Flight Software will meet the objectives listed below.

1) Control the state of the CAPS system.
   - initialize the CAPS system to a default safe state
   - interpret logical telemetry (LTLM) rate commands for SSR data management
   - interpret BIU discrete command bits
   - interpret spacecraft STMs
   - interpret CAPS mode commands
   - reset/release CPU 2
   - provide timing and synchronization with CPU 2.

2) Interface with the Cassini spacecraft (S/C) via the BIU using the MIL STD 1553B bus protocol. The functions of this interface include:
- initialize the BIU
- accept packetized commands on subaddress 7, 8, 9 and 26
- interrogate the BIU discrete command bits
- set the BIU discrete status bits
- packetize (1553B protocol) Housekeeping (HK) and Science (SCI) data for pickup by CDS on subaddress 12 and 11
- store the data in BIU memory for CDS telemetry (TLM) pickup
- monitor and report the status of CAPS S/C communications.

3) Interface with CPU 2 via shared RAM and processor-to-processor interrupts. The functions of this interface include:
- pass CPU 2 specific commands from CDS to CPU 2
- pass CPU 1 generated commands to CPU 2
- read IMS data products
- read B-Cycle header information
- read CPU 2 supplied housekeeping data
- service CPU 2 requests
- set CPU 2 control flags/variables.

4) Interface to the ELS sensor. The functions of this interface include:
- acquire ELS data
- ELS sensor threshold processing
- ELS deadtime correction
- interpret ELS commands and configure the ELS Sensor Management Unit
- produce LTLM dependent ELS data products (16, 8, 4, 2, 1, 0.5 and 0.25 kbps).

5) Interface to the IBS sensor. The functions of this interface include:
- acquire IBS data
- perform IBS sensor threshold processing
- perform IBS deadtime correction
- Interpret IBS sensor commands and configure the IBS sensor
- produce LTLM dependent IBS data products (16, 8, 4, 2, 1, 0.5, 0.25 kbps).

6) Control HV supplies. The control functions include:
- maintain sweep tables
- supply safety
- synchronize/write supply control values.
- provide HV/MCP sensitivity safety monitoring.

7) Interface to the ACT. The functions of this interface include:
- maintain compensation tables
- apply compensation algorithms to microsteps
- synchronize/write ACT microstep values
- read ACT status and position data
- interpret ACT mode commands.

8) Acquire CAPS HK and monitor data:
- control analog-to-digital conversion of monitors
- read sensor status, mode, and control data
- read software counters, statuses, and related data.

9) Format CAPS HK and SCI data:
- packetize the data to CCSDS standard.

10) Produce data products for:
- ELS
- IBS
- Actuator
- Housekeeping
- CPU1 Memory Readout

11) Provide a memory load/patch capability.

12) Provide Assisted Load Block (ALF) capability.

13) Provide Instrument Expanded Blocks (IEB), a.k.a. sequences, capability.

3.1.3 Software System Architecture

The CAPS DPU is a multi-processor based hardware system that distributes loosely coupled, fixed flight software tasks between three 1750A processors designated as CPU 1, CPU 2, and the Spectrum Analyzer Module (SAM). CPU 1 is the "front end" of the DPU and is the only processor in the DPU that communicates with the spacecraft. CPU 1 executes independently of CPU 2 and SAM. CPU 2 and SAM execute in tandem with SAM slaved to CPU 2. SAM calculates ion/molecule data from the TDC/IMS sensor. These results are passed through RAM memory shared between SAM and CPU 2. CPU 2 produces the IMS data products and CPU 2 related housekeeping data. This data is communicated to CPU 1 via RAM memory shared between CPU 1 and CPU 2. CPU 1 transfers the CPU 2 data products to the telemetry stream with the ELS and IBS data products and includes CPU2 housekeeping data in the housekeeping telemetry stream.

CAPS CPU 1 flight software is designed as an interrupt driven data acquisition, control, and telemetry production subsystem. Interrupt routines provide the time-critical foreground processing for the flight system. These routines maintain CAPS sample clock time base and synchronization with the spacecraft, control and monitor actuator movement, acquire science and housekeeping monitor data from the ELS and IBS sensors, coordinate the BIU and CPU 2 interface functions, and provide a watchdog timer function. The CPU 1 flight software main routine provides background processing that includes data compression, data product generation, telemetry formatting and the non-time-critical subset of command execution.

3.1.4 Error Handling Philosophy

When the CAPS flight software encounters an error, the software indicates the error type in the housekeeping stream and continues operations. Error diagnosis and correction is left as a ground function. CAPS is programmed to degrade gracefully and safely if a fatal error is encountered. If a non-fatal error is encountered CAPS will continue to operate to ensure that unaffected science and housekeeping data can still be transmitted.

A hardware watchdog is provided as a safety should the CPU 1 software fail. The 1753 contains a watchdog timer. It is setup for a 32 second period and requires an update to the timer at least once every 32 seconds. After 32 seconds the watchdog timer generates a pulse that is wired into the DPU reset causing a "hard" reset of the entire DPU (CPU1, CPU2, SAM, ELS, IBS, TDC, high voltage supplies).

Before commanding the ELS, IBS, HVU1 and HVU2 power supplies, the flight software verifies the current voltage on the supply matches the voltage commanded by a previous high voltage command. If the voltage does not fall within a tolerance specified in tables within the flight software, the command is rejected and an error bit is set in the CPU 1 error code and reported in housekeeping.

3.2 Flight Software Functional Specifications

3.2.1 Spacecraft Communications

The engineering subsystems and science instruments on the Cassini spacecraft communicate over a MIL-STD 1553B dual redundant bus. The 1553B standard defines an architecture that consists of a single master device (Bus Controller) and one or more slave devices (Remote Terminals). The spacecraft Command and Data Subsystem (CDS) serves as the Bus Controller (BC) and the engineering subsystems and science instruments act as Remote Terminals (RT). Communications occur on the bus in small message blocks (up to 32 data words) as defined in the 1553B standard.

CAPS CPU1 flight software is responsible for handling the MIL-1553 communications as defined by JPL. For details about spacecraft communications requirements see the BIU Design Package (JPL D-9992) Document, Cassini Orbiter Functional Requirements Book, Spacecraft Intercommunications (CAS-3-271), Cassini Orbiter Functional Requirements Book, Telemetry Formats and Measurements (CAS-3-281), and Cassini Orbiter Functional Requirements Book, Uplink Formats & Command Tables (CAS-3-291). See paragraph 4.3.1 BIU for a detailed description of the BIU interface.

3.2.2 System Timing and Synchronization

The following sections describe the timing signals used to coordinate data acquisition, commanding, and telemetry boundaries and the relationship of these signals to the S/C time.

3.2.2.1 RTI

The CDS maintains spacecraft time and provides this time to all users once each second as a regular communication service. The CDS further delineates the passage of time in each second by broadcasting a synchronization message 8 times each second. This synchronization message, known as the Real Time Interrupt (RTI), is slaved to the central CDS timing unit and therefore occurs every 125 msec ± 100 μsec (see Figure 3.2-1). The CDS distributes the RTI signal through a 1553B broadcast mode code (Mode Code 17, Synchronize with Data Word). This results in an interrupt that is processed by the CAPS flight software. See section 4.4.4 for a description of the RTI interrupt. Figure 3.2-1 illustrates the numbering of RTIs within a one second period.

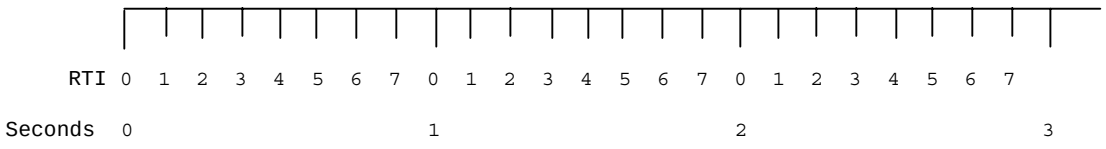


Figure 3.2-1 RTI Timing

3.2.2.2 DTSTART

During each RTI period the CDS provides a dead time start broadcast indicating the beginning of a dead time period on the S/C bus when CDS has completed all bus transactions for the current RTI. Similar to the RTI, CDS distributes this signal through Mode Code 17, Synchronize with Data Word. The dead time start signal (DTSTART) guarantees the instrument a minimum of 5 ms of uninterrupted access to the BIU. The DTSTART may be issued immediately after the RTI if CDS has no bus transactions to perform for the current RTI. The CAPS hardware is designed to generate an interrupt for the DTSTART broadcast. This interrupt has been masked out and

the CAPS flight software does not handle the hardware interrupt. Instead, a 1750A timer is used to generate an interrupt 120 milliseconds after the RTI interrupt. See sections 4.4.3 and 4.4.4 for a description of DTSTART and RTI processing

3.2.2.3 Sample Clocks

CAPS hardware control and data acquisition is based on a 64 second master frame interval slaved to the spacecraft Collection Repeat Cycle. The nominal sample clock timing based on the 64 s master frame is 64.0/1024 = 62.5 ms for IMS, 62.5/2 = 31.25 ms for ELS, and 62.5/8 = 7.8125 ms for IBS. The actuator control frequency is also 7.8125 ms. Figure 3.2-2 shows the relationship of the nominal sample clock signals to the actuator control clock. Each sample clock waveform consists of a deadtime period and a stepping period (also called a data acquisition period).

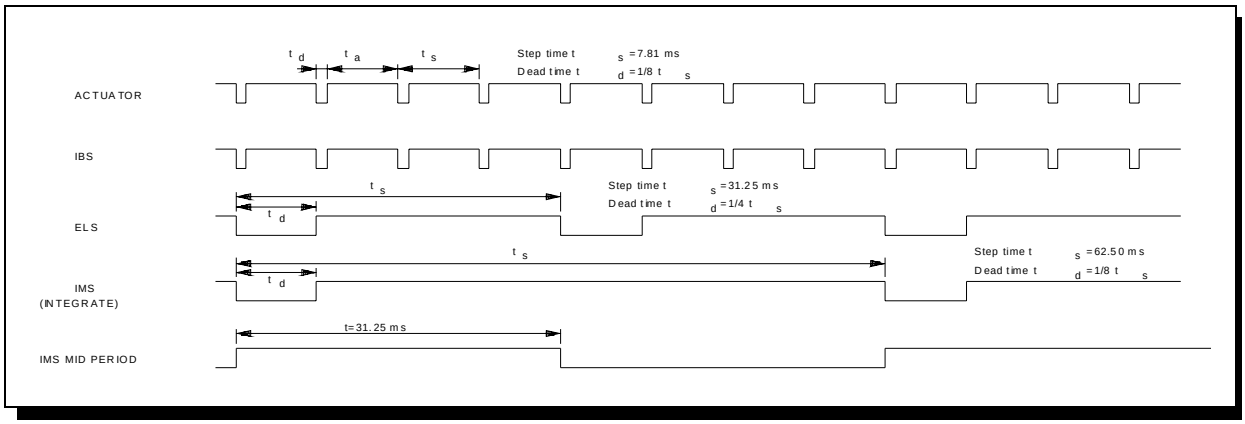


Figure 3.2-2 Sensor Sample Clock Waveforms

Sensor data counters are available to the processor on the falling edge that denotes the start of the deadtime period. Sensor data is read during the deadtime period and stored in RAM for further processing. On the rising edge that denotes the end of the deadtime period and the start of the acquisition period, the sensor electronics accumulates event counts until the start of the next deadtime period. The sample clock intervals can be changed on command (see section 5.8.1.5) to uniformly lengthen all sampling intervals by a factor of x2, x4, or x8.

3.2.2.4 A-Cycle

Acquired sensor data is accumulated over a longer time interval than the sample clock to facilitate the collapsing, compression, and formatting of the science data. The time period over which data from all three sensors can be accumulated is 32 seconds. This time period is designated as an A-cycle. The A-cycle is the time base for creating data products for the ELS and IBS sensors. Some IMS data products are also created on the A-cycle time base.

3.2.2.5 B-Cycle

IMS Time of Flight (TOF) data requires an accumulation period greater than the A-cycle. The B-cycle is defined as this longer accumulation period. A B-cycle is defined as either 8 or 16 A-cycles (256 or 512 seconds) depending upon the current telemetry rate. Reference GSFC document CPU2 Software Functional Design Document for a further discussion of IMS B-Cycles.

3.2.2.6 C-Cycle

IBS operates on an 8-Cycle period. This cycle should not be confused with the IMS B-Cycle. It is independent of the IBS B-Cycle although through the use of B-Cycle commanding it can be synchronized to the IMS B-Cycle. The C-Cycle was introduced to facilitate the new capabilities of IBS, namely solar wind search and track, magnetosphere survey mode and run-length data encoding. See paragraphs 5.5.2 and 5.6.1.2.2 for a description of the new IBS capabilities.

3.2.2.7 Collection Repeat Cycle

The CAPS Collection Repeat Cycle is 64 s or 128 s depending on the spacecraft telemetry mode. CAPS housekeeping is produced on CRC boundaries. Table 3.2-1 lists the CRCs for the various spacecraft telemetry modes.

Table 3.2.1 CDS Version 9 CAPS Collection Repeat Cycles

Mode Name	CRC		Mode Name	CRC	
	HK	SCI		HK	SCI
RTE_5	0	0	S&ER10 (Online)	0	0
RTE_10	64	0	RTE&SPB-14220	64	0.5
RTE_20	64	0	RTE&SPB-22120	64	0.5
RTE_1896	64	0	RTE&SPB-27650	64	0.5
PCHK-24.885	0	0	RTE&SPB-33180	64	0.5
PRLY (Prime)	64	0.5	RTE&SPB-35550	64	0.5
PRLY (Online)	0	0	RTE&SPB-41475	64	0.5
S&ER1	64	0.5	RTE&SPB-47400	64	0.5
S&ER2	64	0.5	RTE&SPB-66360	64	0.5
S&ER3	64	0.5	RTE&SPB-82950	64	0.5
S&ER4	64	0.5	RTE&SPB-99540	64	0.5
S&ER5	64	2	RTE&SPB-110600	64	0.5
S&ER5a	64	2	RTE&SPB-124425	64	0.5
S&ER6	64	1	RTE&SPB-142200	64	0.5
S&ER7	64	0.5	RTE&SPB-165900	64	0.5
S&ER8	64	0.5	SAF-248.85(2)	64	0.5
S&ER10 (Prime)	64	0.5	SAF-142.2	64	4

3.2.2.8 Schedule Repeat Cycle

The Schedule Repeat Cycle (SRC) is defined as the longest collection repeat cycle for any instrument. Spacecraft Telemetry Mode (STM) changes occur on SRC boundaries. The SRCs for all STMs are listed in Table 3.2-2.

Table 3.2.2 CDS Version 9 Cassini Spacecraft Schedule Repeat Cycles

Mode Name	SRC	Mode Name	SRC
RTE_5	8192	S&ER10 (Online)	64
RTE_10	4096	RTE&SPB-14220	64
RTE_1896	64	RTE&SPB-22120	64
PCHK-24.885	64	RTE&SPB-27650	64
PRLY (Prime)	64	RTE&SPB-33180	64
PRLY (Online)	64	RTE&SPB-35550	64
S&ER1	64	RTE&SPB-41475	64
S&ER2	64	RTE&SPB-47400	64

S&ER3	64	RTE&SPB-66360	64
S&ER4	64	RTE&SPB-82950	64
S&ER5	64	RTE&SPB-99540	64
S&ER5a	64	RTE&SPB-110600	64
S&ER6	64	RTE&SPB-124425	64
S&ER7	64	RTE&SPB-142200	64
S&ER8	64	RTE&SPB-165900	64
S&ER9	64	SAF-248.85(2)	64
S&ER10 (Prime)	64	SAF-142.2	64

3.2.2.9 Spacecraft Time

Spacecraft time and telemetry mode information is distributed on BIU subaddress 29 every second during RTI 6. The message is retrieved and processed by CAPS flight software from the BIU during RTI 7. The STM structure is shown in Table 3.2-3. Time and STM updates occur during RTI 7. The NEW_STM_PENDING bit of the STM message is set four seconds before the SRC when an STM change is occurring. This provides CAPS with sufficient notice to prepare for a new physical telemetry rate.

Table 3.2-3 STM Structure

Message Field	Description	Size
Message ID, Delta		
STM Message ID	Bits 8-15 0000 0111B	8 Bits
Time Discontinuity Indicator	Bit 7 1 – time is discontinuous from the last message 0 – time is continuous	1 Bit
New STM Pending	Bit 6 1 – a new STM is pending 0 – no STM change pending	1 Bit
Invalid/Suspect Time	Bit 5 1 – time is invalid because of a cold start and CDS is waiting for ground initialization of time 0 – time is valid	1 Bit
Null Fill	Bit 4-0: all zeros	5 Bits
Current Spacecraft Time MSW	The most significant word of the spacecraft time at the next RTI 0.	1 word
Current Spacecraft Time LSW	The least significant word of the spacecraft time at the next RTI 0.	1 word
Current Science STM	The current spacecraft science telemetry mode.	1 word
Current Engineering STM	The current spacecraft engineering telemetry mode. CAPS does not use this field.	1 word
Next STM/SRC Time	The time of the next schedule repeat cycle. CAPS uses this field modulus 64 to determine its CRC for synchronization.	1 word
Next Science STM	The next spacecraft science telemetry mode. This parameter will differ from Current Science STM when the New STM Pending bit is set.	1 word
Next Engineering STM	The next spacecraft engineering telemetry mode. This parameter will differ from Current Science STM when the New STM Pending bit is set. CAPS does not use this field.	1word

3.2.2.10 Synchronization

The DPU base sample clock is synchronized with the spacecraft during initialization to the first collection repeat cycle or 64 second boundary (see paragraph 3.2.4.1) and every four seconds thereafter. The sample clock is synchronized with the S/C RTI signal. Once synchronized the S/C time is used to time tag CCSDS packets containing housekeeping and science data and to time tag data acquisition.

3.2.3 Telemetry Modes

The CAPS science flight softwarerecognizes the spacecraft telemetry modes listed in Table 3.2-4. The PROM software only recognizes the following STMs: RTE_5, RTE_10, RTE_20, RTE_1896, PCHK-24.885, PRLY, S&ER1, S&ER2, S&ER3, S&ER4, S&ER5, S&ER6, S&ER7, S&ER8, S&ER10. The flight software examines both the science and engineering fields (the first and second word listed in the STM column of the table) in the STM packet.

Table 3.2.4 CDS Version 9 STM Id and Housekeeping Values

Mode Name	STM (hex)	HK Value (hex)	Mode Name	STM (hex)	HK Value (hex)
RTE_5	0300 0303	0	S&ER10 (Online)	0312 0327	N/A
RTE_10	C300 0306	1	RTE&SPB-14220	0321 03B1	10
RTE_20	C300 0309	2	RTE&SPB-22120	0321 03C0	11
RTE_1896	C300 0315	3	RTE&SPB-27650	0321 03C9	12
PCHK-24.885	C000 031E	4	RTE&SPB-33180	0321 03CF	13
PRLY (Prime)	C303 0321	5	RTE&SPB-35550	0321 03D2	14
PRLY (Online)	C303 0321	N/A	RTE&SPB-41475	0321 03D8	15
S&ER1	0306 0324	6	RTE&SPB-47400	0321 03DB	16
S&ER2	0309 0324	7	RTE&SPB-66360	0321 03E4	17
S&ER3	030C 0324	8	RTE&SPB-82950	0321 03EA	18
S&ER4	030F 0324	9	RTE&SPB-99540	0321 03ED	19
S&ER5	0312 0324	A	RTE&SPB-110600	0321 03F0	1A
S&ER5a	0B12 0324	B	RTE&SPB-124425	0321 03F3	1B
S&ER6	0315 0324	C	RTE&SPB-142200	0321 03F6	1C
S&ER7	0318 0324	D	RTE&SPB-165900	0321 03F9	1D
S&ER8	031B 0324	E	SAF-248.85(2)	1327 0342	1E
S&ER10 (Prime)	0312 0327	F	SAF-142.2	0327 0342	1F

3.2.3.1 Physical Versus Logical Telemetry Rates

CAPS has been assigned four physical (S/C) telemetry rates for ICO: 16 kbps 8 kbps, 4 kbps and 2 kbps. The STM determines the physical telemetry rate (see Table 3.2-5). In these S/C telemetry modes the CDS expects to always pick up the same number of science data packets. Logical telemetry rates/modes of 16, 8, 4, 2, 1, 0.5, and 0.25 kbps are defined to provide the data volume management function. The logical data rate commanded must be less than or equal to the physical data rate. Using a “zero length packet” (ZLP), the flight software can provide CDS the required number of packets for a given telemetry rate without taking up space on the SSR. As an example, if the S/C telemetry rate is 16 kbps, CDS expects to pick up two CCSDS packets per second. If CAPS is commanded to the 2 kbps logical telemetry mode, a complete 2 kbps science data stream is sent followed by ZLPs for the remainder of an A-Cycle. This effectively reduces the amount of data stored on the SSR by one-eighth (assuming SSR memory was allocated for S/C telemetry rate of 16 kbps). The science data generated by CAPS at the 2 kbps mode has lower resolution (averaged, summed, compressed) than that produced at the 16 kbps rate.

During STM changes, the flight software will default its logical telemetry rate to lowest of either the current physical rate or the last logical rate. For example:

Scenario 1:

- Current STM SAF 248850, Current Logical TLM is 16 kbps.
- Change to SAF 142200, logical TLM will be 2 kbps
- Change to SAF 248850, logical TLM will be 2 kbps

Scenario 2:

- Current STM is SAF 248850, logical TLM is 0.25 kbps
- Change to SAF 142200, logical TLM will be 0.25 kbps
- Change to SAF 248850, logical TLM will be 0.25 kbps

Table 3.2-5 CDS Version 9 CAPS Science Physical Telemetry Rates

Mode Name	Physical Telemetry Rate (kbps)	Mode Name	Physical Telemetry Rate (kbps)
RTE_5	0	S&ER10 (Online)	0
RTE_10	0	RTE&SPB-14220	16
RTE_20	0	RTE&SPB-22120	16
RTE_1896	0	RTE&SPB-27650	16
PCHK-24.885	0	RTE&SPB-33180	16
PRLY (Prime)	16	RTE&SPB-35550	16
PRLY (Online)	0	RTE&SPB-41475	16
S&ER1	16	RTE&SPB-47400	16
S&ER2	16	RTE&SPB-66360	16
S&ER3	16	RTE&SPB-82950	16
S&ER4	16	RTE&SPB-99540	16
S&ER5	4	RTE&SPB-110600	16
S&ER5a	4	RTE&SPB-124425	16
S&ER6	8	RTE&SPB-142200	16
S&ER7	16	RTE&SPB-165900	16
S&ER8	16	SAF-248.85(2)	16
S&ER10 (Prime)	16	SAF-142.2	2

3.2.3.2 Data Volume Management

Each instrument has been assigned an amount of SSR space to be used to store science and housekeeping telemetry. CAPS has been assigned 14745 blocks (230 kwords of data) of SSR storage for ALF loads and a variable number of blocks for science and housekeeping. During Saturn tour, downlink will be possible for only a few days during each orbit. Science and housekeeping collected during the remaining orbit must be stored on the SSR. Since CAPS will be assigned a fixed portion of SSR space, that space must be managed to ensure science is not lost during more interesting parts of the orbit. The use of logical telemetry rates is the mechanism by which CAPS manages SSR space. CAPS can be programmed to generate lower logical telemetry rates during the less interesting parts of the orbit using up less SSR space and higher logical telemetry rates during the more interesting parts of the orbit when collection of the maximum allowable science data is desired.

3.2.4 Operational Modes

Figure 3.2-3 illustrates the CAPS flight software operational modes. ROM sourced modes are those modes supported by the flight software programmed into PROM. SSR/ground sourced modes are those modes supported by the flight science software. Details of each mode are discussed in the following paragraphs.

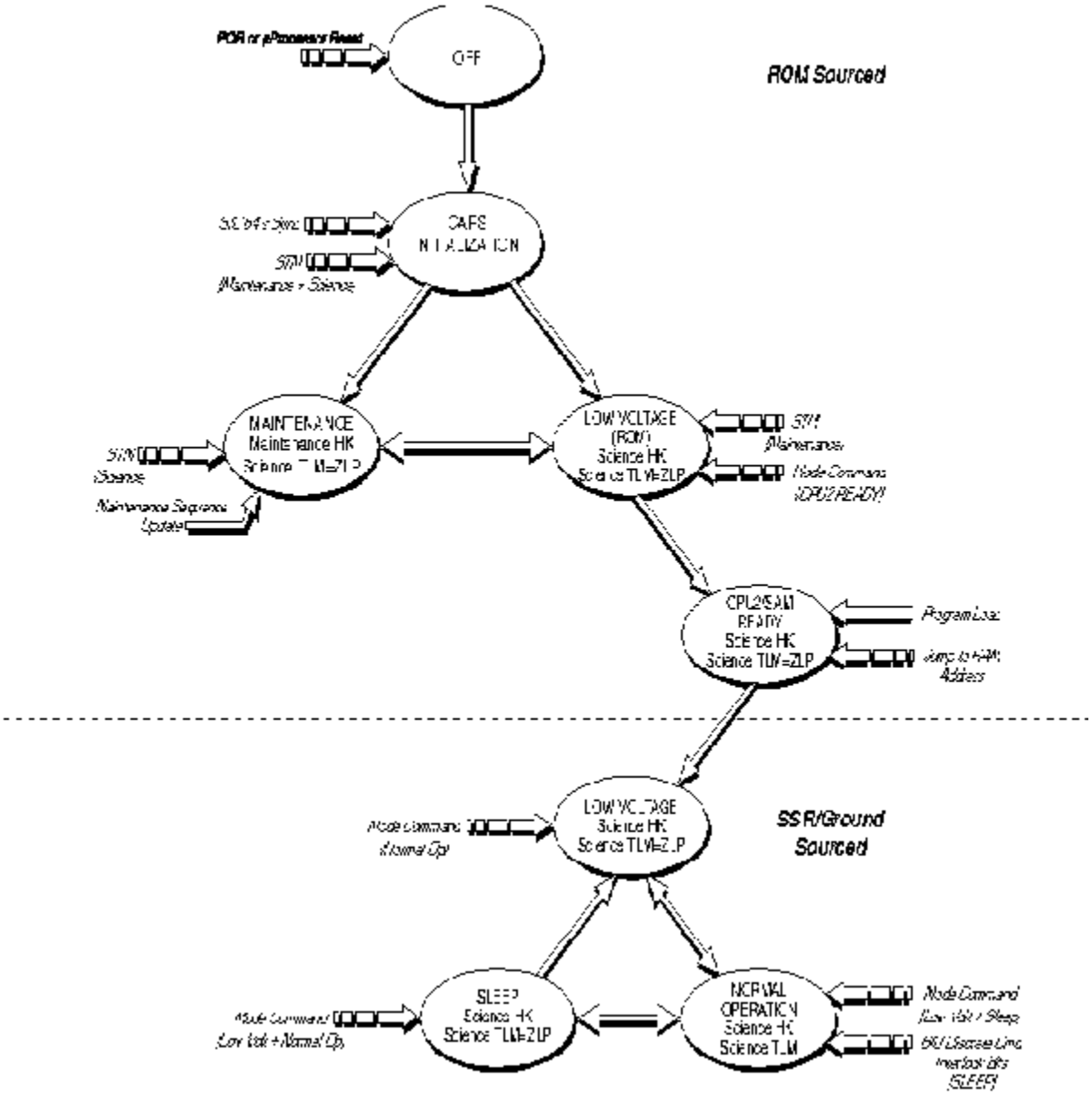


Figure 3.2-3 CAPS Functional State Diagram

3.2.4.1 Initialization

Upon power-up, CPU 2 and SAM are held in reset and CPU 1 begins execution. CPU 1 executes a boot-strap load program that performs a destructive RAM test of local and shared RAM. The results of these tests are reported in the BIU discrete bits (see Table 3.2-6). It then decompresses and writes the ROM based flight software to RAM starting at a predefined location. As it decompresses the flight software it performs a checksum. The location the software is loaded can be changed in flight by setting bit 3 in the BIU discrete command bits using the command 82RT_ARADDR. A 0 in this bit will load the flight software at 0x80000. A 1 in this bit will load the flight software at 0x90000. This capability is provided should the RAM from 0x80000 to 0x8FFFF fail.

Table 3.2-6 BIU Discrete Status Bit Assignments

Discrete Status Bit	State/Description
15 – Executing in ROM	0 – Flight software executing out of ROM
	1 – Flight software executing out of RAM
14 – Boot Complete/BIU Initialized	0 – Flight software boot not complete
	1– Flight software boot complete; BIU initialized
13 – PROM Test Status	0 – PR0M test passed
	1 – PROM Test Failed
12 – RAM Test Status	0 – RAM test passed
	1 – RAM test failed
11– Shared RAM Test Status	0 – Shared RAM test passed
	1 – Shared RAM test failed
10 - 0 – Not Used	

This decompressed and relocated code (PROM code) then initializes CAPS hardware. The BIU autoinitializes upon power-up with a default table that allows limited bus services. CPU 1 must define the BIU tables and pointers required to fully communicate over the 1553B bus (see Appendix H). CPU 1 then sets the BIU discrete status bits indicating the BIU descriptor tables have been initialized and CPU 1 is executing out of RAM. CPU 1 then initializes the interrupt table and pointers. CPU 1 initializes hardware and software latches and counters to their initial states and waits for the Spacecraft Telemetry Mode (STM) packet from the CDS that corresponds to the next collection repeat cycle boundary (64 second boundary). At the 64 second sync boundary CPU 1 initiates the hardware clock that provides all timing signals used by CAPS. In this manner CAPS synchronizes to the S/C time base. CPU 1 then enters either the Maintenance Mode or the Low Power (ROM) Mode depending on the STM.

3.2.4.2 Maintenance Mode

The spacecraft no longer supports the IM_40 or IM_40_ALT1 STMs. This mode is no longer available. Since this mode is supported by the onboard PROM software, the following discussion remains for historical purposes.

In this mode CPU 1 produces maintenance housekeeping telemetry packets and zero length science packets. A subset of the CAPS command list is recognized in this state. The subset includes commands to release the ACT launch latch and the IMS cover. It also includes commands required to perform maintenance cycling of the actuator and ALF commands destined for CPU 1. See Appendix N for a list of valid commands by mode. CAPS will remain in this mode until a new STM is received that indicates the S/C is entering a science telemetry mode. If the STM is changed by the S/C to a science telemetry mode CAPS enters the Low Power (ROM) mode.

3.2.4.3 Low Power (ROM) Mode

When the STM indicates that the S/C telemetry mode is science while CPU 1 is initializing or is in Maintenance Mode and the STM transitions to a science telemetry mode, the Low Power (ROM) Mode is entered. In this mode CPU 1 produces science (normal) format housekeeping telemetry packets and zero length science

packets. CPU 1 can also be commanded to produce maintenance format housekeeping telemetry packets. In this mode CPU 2 and SAM are still held in reset, the high voltage supplies are off, and the ACT, IBS, and ELS are off. This is the lowest power state of CAPS for any of the normal modes (Low Voltage, CPU 2/SAM Ready, Normal Science, and Sleep modes). A subset of the CAPS command list is recognized in this mode. The subset includes ALF commands destined for CPU 1, CPU 2, DPU mode, and maintenance ACT commands. It also includes commands to release the ACT launch latch and the IMS cover. See Appendix N for a list of valid commands by mode. Only the Maintenance and the CPU 2/SAM Ready modes are valid transition modes from Low Power (ROM) mode.

3.2.4.4 CPU 2/SAM Ready Mode

In this mode, CPU 2 is released from reset and begins executing its PROM software. All commands supported in Maintenance Mode and Low Power Mode (ROM sourced) are supported, except IMS cover and ACT commands. In addition, CPU 2 commands that are valid for CPU2 PROM and ALF commands destined for CPU 2 are accepted. See Appendix N for a list of valid commands by mode. This mode is designed to be used to load flight science software and transition to Low Power mode (SSR sourced).

3.2.4.5 Low Power (SSR sourced) Mode

In this mode, CPU 2 and SAM are held in reset. The actuator , ELS and IBS are off. High voltage supplies are also off. CPU 1 is producing science (normal) format housekeeping telemetry packets and zero length science packets. This is the lowest power state of the flight science software. Only a subset of CAPS commands are recognized in this mode. Sensor and power supply specific commands are not accepted in this mode. See Appendix N for a list of valid commands by mode.

3.2.4.6 Normal Science Mode

In this mode, CPU2 and SAM have been released from reset and are executing flight science software. Upon entering the mode, ELS, IBS, HVU-1, HVU-2 and ACT are disabled. All commands supported by flight science software are available. In this mode CPU 1 produces science (normal) format housekeeping telemetry packets and science data packets.

3.2.4.7 Sleep Mode

In this mode, CPU2 and SAM have been placed in reset. The sweeping of high voltage supplies is stopped. The actuator is parked and disabled. CPU 1 produces science (normal) format housekeeping packets and zero length science packets. This mode is intended to be a lower power mode from normal science, but without the start up cost of transitioning from Low Power to Normal Science. The ELS MCP, IMS ST, LEF, Retard, Accelerate, and IBS CEM supplies are left at their programmed levels.

3.2.4.8 CAPS Mode Summary

Table 3.2-7 summarizes the CAPS modes.

Table 3.2-7 State Transition Matrix S/C Science Telemetry Mode

TO	*FROM*					
	Maintenance (No longer available, historical only)	Low Voltage (PROM)	Low Voltage (SSR Sourced)	CPU2/SAM Ready	Normal Science	Sleep
Maintenance (No longer available, historical only)	N/A	Produce Maintenance HK	Illegal	Illegal	Illegal	Illegal
Low Voltage (PROM)	Produce Science HK	N/A	Illegal	Illegal	Illegal	Illegal
Low Voltage (SSR Sourced)	Illegal	Illegal	N/A	Reset CPU2 "Jump" to CPU1 RAM Exec Address Supplemental Heater ON	Reset CPU2 Supplemental Heater ON HV +15V OFF ACT Park and Disable SCI = ZLP	HV +15V OFF Supplemental Heater ON
CPU2/SAM Ready	Illegal	Release CPU 2 Wait for ALF blocks, RAM Exec, or DPU Mode command	Illegal	N/A	Illegal	Illegal
Normal Science	Illegal	Illegal	Release CPU2 Send CPU2_RAM_EXEC Supplemental Heater OFF HV cmds allowed Sensor cmds allowed ACT cmds allowed (if RT opmode = OPWART) SCI = data prod. Packets	Illegal	N/A	Release CPU2 Supplemental Heater OFF HV sweep cmds allowed ACT cmds allowed (if RT opmode = OPWART) SCI = data prod. Packets
Sleep	Illegal	Illegal	Illegal	Illegal	CPU2 reset ELS Mode A ACT Park and Disable HV ON Sweeping disabled HV sweep cmds disabled ACT cmds disabled SCI = ZLP	N/A

Table 3.2-8 CAPS Power Allocation

CAPS Mode	Power Allocation
Maintenance	14.3 W
Low Power (ROM)	14.3 W
CPU 2/SAM Ready	14.3 W
Low Power (SSR Sourced)	14.3 W
Normal Science (OP)	18.0 W
Normal Science (OPWART)	21.0 W
Sleep	13.2 W

3.2.5 Commands

CAPS commands are divided into two basic types: Inter-processor commands and Instrument Commands. Instrument Expanded Blocks (IEB) or distributed sequences are instrument commands that are stored in CAPS RAM and executed according to a time tag.

3.2.5.1 Inter-processor Commands

Inter-processor commands are those commands that are internal to CAPS and are passed between CPU 1 and CPU2. They are used to communicate control information between CPU 1 and CPU 2. Commands can be passed from CPU 1 to CPU 2 and from CPU 2 to CPU 1. Tables 3.9-1 and 3.9-2 list the Inter-processor commands. Inter-processor commands are discussed in greater detail in paragraph 5.8.3.

Table 3.2-9 CPU1 to CPU2 Inter-processor Commands

Command	Description
Data Rate Change	This command notifies CPU 2 of a logical telemetry rate change. It is sent to CPU 2 62.5 milliseconds before the beginning of an A-Cycle
Read Command List	This command notifies CPU 2 of instrument commands in its command list.

Table 3.2-10 CPU 2 to CPU 1 Inter-processor Commands

Command	Description
B-Cycle Starting	This command notifies CPU 1 that a B-Cycle is beginning at the next sample clock interrupt.
Process Background	This command notifies CPU 1 to perform background processing.
Shared RAM Fail	This command notifies CPU 1 that CPU 2 has detected a shared RAM failure.
Shared RAM Pass	This command notifies CPU 1 that CPU 2 shared RAM test passed.
SAM RAM Fail	This command notifies CPU 1 that CPU 2 has detected a SAM RAM failure.
SAM RAM Pass	This command notifies CPU 1 that CPU 2 SAM RAM test passed.
RAM Fail	This command notifies CPU 1 that CPU 2 has detected a local RAM failure.
RAM Pass	This command notifies CPU 1 that CPU 2 local RAM test passed.
Threshold Exceeded	This command notifies CPU 1 that CPU 2 data counts have exceeded the threshold established by 82DPU_THRESHOLD.

3.2.5.2 Instrument Commands

Instrument commands are ground based commands. They can be received by the spacecraft from the ground and sent immediately to CAPS or stored as part of CDS sequences. Basically, these are commands received in BIU subaddresses 7, 8 or 9. They can be executed immediately upon receipt, deferred until an A-Cycle boundary, or deferred until a B-Cycle boundary. Paragraph 5.8.1 discusses each of the CPU 1 instrument commands in greater detail. Appendix N lists the CAPS instrument commands.

3.2.5.3 Instrument Expanded Blocks

Instrument Expanded Blocks (IEB) or distributed sequences are instrument commands that are stored in CAPS RAM and executed according to a time tag. All instrument commands are supported in IEB's with the exception of 82RT* commands. These commands are processed by the BIU directly. Although, the FSW does not prevent the execution of 82MEM* commands, 82SEQ_LOAD, 82SEQ_BLOCK, 82SEQ_CHECKSUM and 82 TRIGGER, it is recommended these commands **not** be executed from an IEB. CAPS science software currently supports 85 sequences:

Table 3.2-11 IEB Configuration

IEB Number	Description	Size (words)
0	Master IEB #1	1024
1	Master IEB #2	1024
2	Observation IEB #1	64
3	Observation IEB #2	64
4	Observation IEB #3	64
5	Observation IEB #4	64
6	Observation IEB #5	64
7	Observation IEB #6	64
8	Observation IEB #7	64
9	Observation IEB #8	64
10	Observation IEB #9	64
11	Observation IEB #10	64
…		64
58	Observation IEB #57	64
59	Observation IEB #58	64
60	Observation IEB #59	64
61	Observation IEB #60	64
62	Survey Mode IEB #1	128
63	Survey Mode IEB #2	128
64	Survey Mode IEB #3	128
65	Survey Mode IEB #4	128
66	Survey Mode IEB #5	128
67	Survey Mode IEB #6	128
68	Survey Mode IEB #7	128
69	Survey Mode IEB #8	128
70	Survey Mode IEB #9	128
71	Survey Mode IEB #10	128
72	Survey Mode IEB #11	128
73	Survey Mode IEB #12	128
74	Survey Mode IEB #13	128
75	Survey Mode IEB #14	128
76	Survey Mode IEB #15	128
77	Survey Mode IEB #16	128
78	Survey Mode IEB #17	128
79	Survey Mode IEB #18	128
80	Survey Mode IEB #19	128
81	Survey Mode IEB #20	128
82	Mode Transition IEB - Low Power to Normal Science	256
83	Mode Transition IEB - Normal Science to Low Power	256
84	Mode Transition IEB – Normal Science to Sleep	256

85	Mode Transition IEB – Sleep to Normal Science	256
86	Mode Transition IEB – Sleep to Low Power	256
	Total IEB Space (words)	9792

A sequence can be triggered with the 82TRIGGER command or internally with a 82SEQ_LINK command. A mode transition sequence is automatically triggered by the flight software when an instrument mode transition occurs. The mode transitions are listed in Table 3.2-11. The mode is set either before or after the mode transition occurs, depending on the commands that will executed during the mode transition. For example, from low power to normal science, the mode is set to normal science and the MTS is triggered. This allows normal science commands that are illegal during low power to be executed.

4 HARDWARE FUNCTIONAL DESIGN DESCRIPTION

4.1 Overview

CAPS consists of three PACE 1750A microprocessors. They are labeled CPU 1, CPU 2 and SAM. CPU1 is responsible for interfacing to:

- The actuator (ACT)
- The actuator launch latch thermal wax actuator.
- The spacecraft via Bus Interface Unit (BIU)
- The Electron Spectrometer (ELS) sensor
- The High Voltage Unit 1 (HVU-1)
- The High Voltage Unit 2 (HVU-2)
- The Ion Beam Spectrometer (IBS) sensor
- The Ion Mass Spectrometer (IMS) cover thermal wax actuator

CPU 1 interfaces to CPU 2 through a common shared memory. CPU 1 interfaces with the ACT, BIU, ELS, HVU-1, HVU-2 and IBS via an address/data control bus. CPU 2 interfaces with the SAM and the TDC via an address/data control bus. All interfaces are memory mapped. A general block diagram of the DPU configuration is shown in Figure 4.1-1.

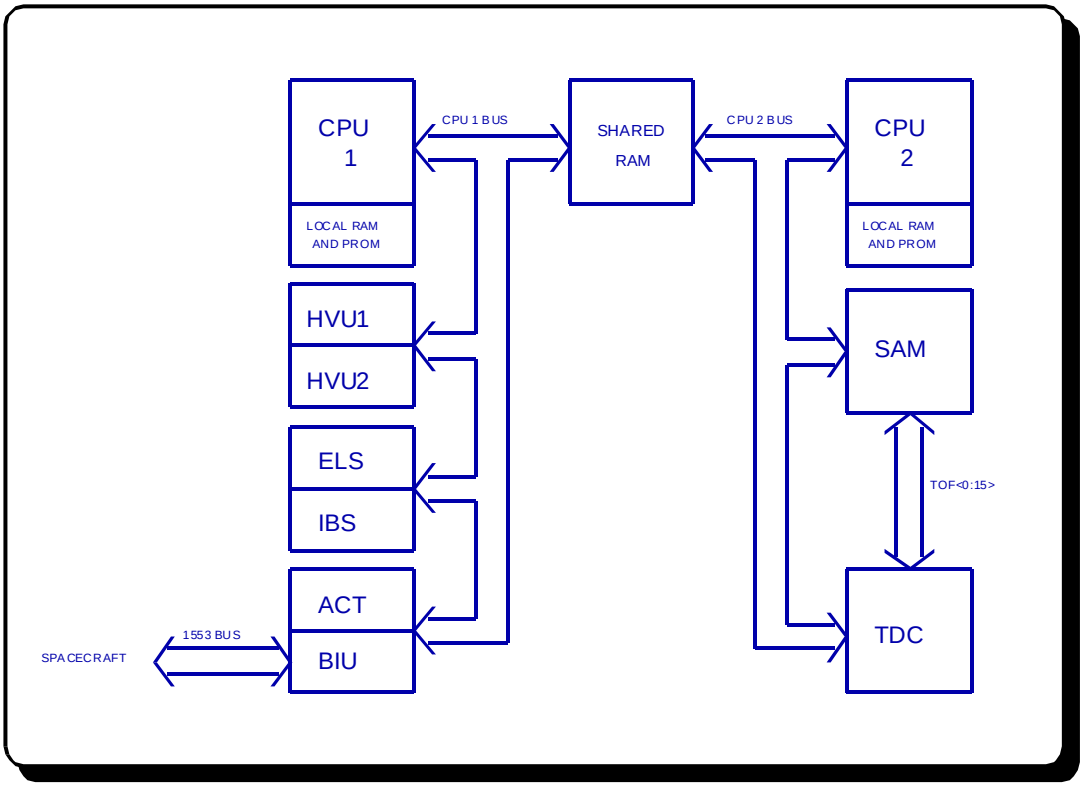


Figure 4.1-1 DPU Configuration

4.2 Memory Organization

Memory allocated to CPU 1 is mapped over four 256k word memory partitions (MEMQ1 to MEMQ4). The assignments within a memory partition are partially dictated by the speed of the memory mapped device(s) mapped into the partition. Partitions are divided into subpartitions. Table 4.2-1 lists the CPU 1 memory partitions/subpartitions with address ranges and provides descriptive tables for the memory mapped I/O boards.

Table 4.2-1 CPU 1 Memory Organization

Partition	Address Range	Size (words)	S/W Wait States	Description
MEMQ4	C0000-FFFFF	256K	1	Shared RAM Memory
MEMQ3	80000-BFFFF	256K	0	Local RAM Memory
MEMQ2	70000-7FFFF	64K	2	BIU Memory
	60000-6FFFF	64K		BIU Registers
	50000-5FFFF	64K		Reserved
	40000-4FFFF	64K		HVUBD Control
MEMQ1	38000-3FFFF	32K	1	HVU-2 Control
	30000-37FFF	32K		IBSELSBD Control
	28000-2FFFF	32K		IBS Control
	20000-27FFF	32K		BIUBD
	18000-1FFFF	32K		CPU 2 IRQ
	10000-17FFF	32K		CPU 1 Control Regs.
	00000-0FFFF	64K		CPU 1 ROM Memory

4.2.1 ROM Memory

CPU 1 memory organization allows up to 64k words of PROM. Board space limitations create a trade-off between the amount of ROM and RAM that actually populates the memory board. The CPU 1 board is populated with 16k of PROM. The CAPS PROM code fits within this 16k of PROM. The CPU 1 PROM contains the software modules required to bootstrap code into RAM, perform initialization of the BIU and CAPS hardware, perform the functions defined for the Maintenance, Low Voltage (ROM), and CPU 2/SAM Ready modes.

4.2.2 Local RAM Memory

CPU1 contains 256k words of local RAM beginning at physical address 0x80000 through 0xBFFFF. Table 4.2-2 lists the major segments of CPU 1 Local RAM.

Table 4.2-2 CPU 1 RAM Layout

RAM Segment	Description
0x80000 – 0x95FFF	CPU 1 program space
0x96000-0x9FFFF	IBS Acquisition/Compression Buffers
0xA0000 – 0xA7FFF	ELS Acquisition/Buffers
0xA8000 – 0xB3FFF	CPU 1 data space
0xB4000 – 0xB6FFF	Free
0xB7000 – 0xB7FFF	PROM/RAM global data
0xB8000 – 0xBCFFF	Free
0XBD000 – 0xBFFFF	Instrument Expanded Blocks

4.2.3 Shared RAM Memory

The communication interface between CPU 1 and CPU 2 will be shared memory. Shared memory is physically located on the CPU2 board. 256K of shared memory is available starting at physical address 0xC0000 through 0xFFFFF. See document 5548-FSFD-02 Cassini CAPS CPU 2 Flight Software Functional Design Document for a description of the contents of shared memory. The lower portion of shared memory is used by CPU1 and CPU2 to communicate. This is followed by the IMS group tables. SwRI shall maintain configuration control of the processor-to-processor shared memory interface.

4.3 Hardware Operation

The following sub-paragraphs describe the various CAPS subsystems. These include:

- MIL-STD-1553B Bus Interface Unit
- Ion Beam Spectrometer Sensor Interface
- Electron Spectrometer Sensor Interface
- Actuator Motor Interface and Launch Latch
- High Voltage Unit #1 Interface
- High Voltage Unit #2 Interface
- IMS Cover Launch Latch Mechanism

4.3.1 Bus Interface Unit

The CAPS BIU serves as a Remote Terminal on the 1553B bus providing the interface between the CDS and CAPS. It is a dual-redundant bi-directional serial bus that is fully MIL-STD-1553B compliant. The CAPS BIU is configured as a 1553B remote terminal and is embedded in the CAPS DPU. CDS communicates with CAPS by referencing CAPS' remote terminal address 6.

4.3.1.1 BIU Registers

The BCRTM control registers can be accessed by CPU 1 allowing the software control of the BCRTM processing. There are 18 control registers in the BCRTM. Table 4.3-1 presents the memory map for the BIU registers.

Table 4.3-1 BIU Registers Memory Map

Register	Address	R/W	Description
Control	60000	R/W	During initialization the value 0181 hex is stored in this register.
Status	60001	R/W	This registers reflects the status of the BCRTM. It is used during BIU initialization to determine the state of BIU reset and built-in-test.
Current Command Block	60002	R/W	This register contains the pointer to command block being executed.
Polling Compare Register	60003	R/W	This register is not used by CAPS flight software.
Built-In-Test Register	60004	R/W	This register returns the results of the BCRTM built-in-test. This is reported in housekeeping as BIU Auto Init. A value in this register other than zero indicates a failure.
Current Command Register	60005	R/W	This register is not used by CAPS flight software.
Interrupt Log List Register	60006	R/W	This register contains the pointer to the interrupt log list
High Priority Interrupt Enable Register	60007	R/W	This register is used to enable high priority interrupts. CAPS does not uses high priority interrupts.
High Priority Interrupt Status Register	60008	R/W	This register is not used by CAPS flight software.
Standard Interrupt Enable Register	60009	R/W	This register is used to enable standard interrupts. CAPS does not uses standard interrupts.
Remote Terminal Address Register	6000A	R/W	This register is not used by CAPS flight software. The CAPS remote terminal address is fixed in hardware.
BIT Start Register	6000B	R/W	Writing to this register causes the BCRTM built-in-test to be executed.
Programmed Reset Register	6000C	R/W	Writing to this register causes a reset of the BCRTM.
RT Timer Reset Register	6000D	R/W	This register is not used by CAPS flight software.
Bus Monitor Control Register	6000E	R/W	This register is not used by CAPS flight software.
Reserved	6000F	R/W	This register is not used by CAPS flight software.
Monitor Selected Remote Terminal Addresses 15-0	60010	R/W	This register is not used by CAPS flight software.
Monitor Selected Remote Terminal Addresses 16-31	60011	R/W	This register is not used by CAPS flight software.

4.3.1.2 BIU Memory Map

CAPS communication with the BIU consists mainly of reading data blocks out of or writing data blocks into the BIU's memory. The BIU houses two 8K x 8 static RAMs used to store science and housekeeping data as well as the 1553B remote terminal descriptor tables and other 1553B message or status information and data. Table 4.3-2 presents the memory structures map for the BIU memory. CAPS cannot write to BIU memory locations 70000h to 7013Fh. These locations are reserved specifically for the Auto-initialization Descriptor Table. Attempted writes to these locations do not change the contents of memory and causes the BIU's Write Protection Violation (WP_VILTN) output to go high.

Auto-initialization Descriptor Table

On power-up or after certain resets, the BIU goes through auto-initialization. During auto-initialization the BIU ASIC loads the lower 320 words of memory with a BCRTM Descriptor Table that gives the BIU a basic set of communications capabilities. This area of memory is not write-accessible by CAPS.

Auto-initialization Data and Lists

Following auto-initialization, this area of memory is used for data and lists until CAPS configures the BIU for its specific communications needs. This area provides the basic communications services.

CAPS Descriptor Tables

Descriptor Tables are 320 word tables composed of 4-word entries that determine the BCRTM's response to each type of Subaddress and Mode Code. There is a table entry for all receive subaddress 1-31, transmit subaddress 1-31 and mode codes 0-31. These tables are loaded by CAPS as part of its initialization process. Descriptor Tables must be placed on 512-word boundaries of the BIU memory map. Two sets of Descriptor Tables, Message Status Word Lists, Receive Data areas, and Transmit Data areas are required to perform double buffering of BIU input/output. Figure 4.3-1 illustrates the relationship between a descriptor table entry and the transaction list and status list. Table 4.3-3 lists the contents of a descriptor table. Tables 4.3-4 and 4.3-5 describe the contents of the descriptor table entry.

Table 4.3-2 BIU Structures Memory Map

Structure Name	Address Range
Auto-initialization Table	70000-701FF
Auto Initialization Data	70200-703FF
CAPS Descriptor Table 1	70400 – 705FF
CAPS Descriptor Table 2	70600 – 707FF
CAPS Status Lists	70800-709C9
Transmit Data Buffer 1	709CA-70E2A
Transmit Data Buffer 2	709E2B-7128B
Received Data Buffer 1	7128C-718D5
Received Data Buffer 2	718D6 – 71F1D
Interrupt Log List	71F1E – 71F20
Phantom RAM	72000-77983
RTI/DTSTART	77984
Phantom RAM	77985-7DFFF
Discrete Commands/Status	7E000-7E002
Phantom RAM	7E003-7FFFF

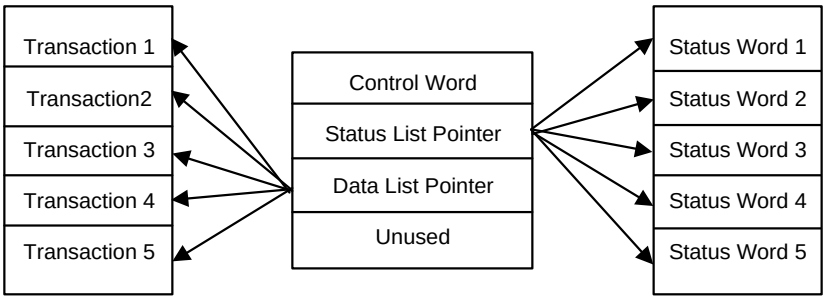


Figure 4.3-1 Descriptor Table Relationships

Table 4.3-3 Descriptor Table Layout

Descriptor Table Function	Offset Within Table (hex)	Description
Receive Subaddress 1	0	BIU Boot Kernel
Receive Subaddress 2	4	BIU Memory Load
Receive Subaddress 3	8	Discrete Commands
Receive Subaddress 4	C	Not Used
Receive Subaddress 5	10	Not Used
Receive Subaddress 6	14	Not Used
Receive Subaddress 7	18	Noncritical Commands
Receive Subaddress 8	1C	Critical Commands
Receive Subaddress 9	20	Fault Protection Commands
Receive Subaddress 10	24	Ancillary Data Broadcast
Receive Subaddress 11	28	Reserved
Receive Subaddress 12	2C	Reserved
Receive Subaddress 13	30	Reserved
Receive Subaddress 14	34	Reserved
Receive Subaddress 15	38	Reserved
Receive Subaddress 16	3C	Reserved
Receive Subaddress 17	40	Reserved
Receive Subaddress 18	44	Reserved
Receive Subaddress 19	48	Not Used
Receive Subaddress 20	4C	Not Used
Receive Subaddress 21	50	Not Used
Receive Subaddress 22	54	Reserved
Receive Subaddress 23	58	Reserved
Receive Subaddress 24	5C	Reserved
Receive Subaddress 25	60	Reserved
Receive Subaddress 26	64	Reserved
Receive Subaddress 27	68	Reserved
Receive Subaddress 28	6C	Reserved
Receive Subaddress 29	70	Telemetry Mode & Time Broadcast
Receive Subaddress 30	74	BIU Data Wraparound Test
Receive Subaddress 31	78	Indicates a Mode code
Unused	7C	Unused
Transmit Subaddress 1	80	BIU Boot Kernel Read Back
Transmit Subaddress 2	84	BIU Memory Read Back

Transmit Subaddress 3	88	Discrete Status Read Back
Transmit Subaddress 4	8C	Not Used
Transmit Subaddress 5	90	Not Used
Transmit Subaddress 6	94	Not Used
Transmit Subaddress 7	98	Noncritical Command Read Back
Transmit Subaddress 8	9C	Critical Command Read Back
Transmit Subaddress 9	A0	Fault Protection Command Read Back
Transmit Subaddress 10	A4	Ancillary Data Pickup
Transmit Subaddress 11	A8	CCSDS Science Packet Pickup
Transmit Subaddress 12	AC	CCSDS Housekeeping Packet Pickup
Transmit Subaddress 13	B0	Reserved
Transmit Subaddress 14	B4	Not Used
Transmit Subaddress 15	B8	Not Used
Transmit Subaddress 16	BC	Not Used
Transmit Subaddress 17	C0	Not Used
Transmit Subaddress 18	C4	Not Used
Transmit Subaddress 19	C8	Not Used
Transmit Subaddress 20	CC	Not Used
Transmit Subaddress 21	D0	Not Used
Transmit Subaddress 22	D4	Reserved
Transmit Subaddress 23	D8	Service Requests
Transmit Subaddress 24	DC	Heartbeat Collection
Transmit Subaddress 25	E0	Fault Protection Data
Transmit Subaddress 26	E4	Reserved
Transmit Subaddress 27	E8	Reserved
Transmit Subaddress 28	EC	Reserved
Transmit Subaddress 29	F0	Telemetry Mode/Time Read Back
Transmit Subaddress 30	F4	BIU Data Wraparound Read Back
Transmit Subaddress 31	F8	Indicates a Mode Code
Unused	FC	Unused
Mode Code 0 & 16	100	Dynamic Bus Control & Transmit Vector Word
Mode Code 1 & 17	104	Synchronize w/o And With Data Word
Mode Code 2 & 18	108	Transmit Status Word & Transmit Last Command
Mode Code 3 & 19	10C	BIT and Transmit BIT
Mode Code 4 & 20	110	XMTR Shutdown & Selected XMTR Shutdown
Mode Code 5 & 21	114	Override XMTR Shutdown & Override Selected XMTR Shutdown
Mode Code 6 & 22	118	Inhibit Terminal Flag & Reserved
Mode Code 7 & 23	11C	Override Inhibit Terminal Flag & Reserved
Mode Code 8 & 24	120	Reset Remote Terminal & Reserved
Mode Code 9 & 25	124	Not Used
Mode Code 10 & 26	128	Not Used
Mode Code 11 & 27	12C	Not Used
Mode Code 12 & 28	130	Not Used
Mode Code 13 & 29	134	Not Used
Mode Code 14 & 30	138	Not Used
Mode Code 15 & 31	13C	Not Used

Table 4.3-4 Subaddress Descriptor Table Entry

Control Word	
Bit Number	Description
15-11	Reserved. These bits are set to zero.
10	Illegal Broadcast Subaddress. Set to indicate to the BCRTM not to access this subaddress with a broadcast command. The Message Error bit in the 1553 status word is set.
9	Illegal Subaddress. Set to indicate to the BCRTM that a command with this subaddress is illegal. The Message Error bit in the 1553 status word is set.
8	Interrupt Upon Valid Command Received. This bit is set to zero for CAPS
7	Interrupt When Index 0. This bit is set to zero for CAPS
6-0	Index. These bits are for indexed message buffering. They are initialized with the maximum number of 1553 messages that can be received by the subaddress. For each 1553 packet received, the index is decremented. By subtracting the index from maximum number of messages expected, the number of messages received can be determined.
Status List Pointer This field contains a pointer (relative to the start of BIU memory) to the start of the status list.	
Data List Pointer This field contains a pointer (relative to the start of BIU memory) to the start of the data area. The BCRTM stores data in RAM beginning at the address indicated by this field. The Data List Pointer is updated by the BCRTM at the end of each successful transaction to point to the start of the next transaction.	
Unused This field is set to zero.	

Table 4.3-5 Mode Code Descriptor Table Entry

Control Word	
Bit Number	Description
15	Interrupt on Reception of Mode Code (without Data Word). This bit is set to 0.
14	Illegalize Broadcast Mode Code (without Data Word).
13	Illegalize Mode Code (without Data Word).
12	Reserved. This bit is set to 0.
11	Illegalize Broadcast Mode Code (with Data Word).
10	Illegalize Transmit Mode Code (with Data Word).
9	Illegalize Receive Mode Code (without Data Word).
8	Interrupt on Reception of Mode Code (with Data Word). This bit is set to 0.
7	Interrupt if Index = 0. This bit is set to 0.
6-0	Index. This field is always zero.
Status List Pointer This field contains a pointer (relative to the start of BIU memory) to the start of the status list.	
Data List Pointer This field contains a pointer (relative to the start of BIU memory) to the start of the data area. The BCRTM stores data in RAM beginning at the address indicated by this field. The Data List Pointer is updated by the BCRTM at the end of each successful transaction to point to the start of the next transaction.	
Unused This field is set to zero.	

Table 4.3.6 Message Status Word Definition

Bit	Description
15	Subsystem Fail Input was asserted during this message
14	Message was broadcasted
13	An error was detected in the message
12-8	Words in the message
7-0	Time tag the message was received.

Transmit Data Buffers

Transmit Data is data that is placed in memory by CAPS for eventual pick-up by the CDS. Descriptor tables contain information that tells the BCRTM where to retrieve data in BIU memory for each Subaddress and Mode Code type. CCSDS Science Packets generated by CAPS are a type of transmit data.

Received Data

Receive Data is data that is sent by CDS to the BIU for eventual retrieval by CAPS. Descriptor Tables contain information that tells the BCRTM where to place data in BIU memory for each Subaddress and Mode Code type. Commands are a type of receive data.

Status Word Lists

For each CDS Bus Message that the BIU handles, the BCRTM generates a Message Status Word. The Message Status Word indicates the type of message (normal or broadcast), the number of data words in the message (up to 32), the approximate time elapsed since the last reset of a BCRTM timer, and error conditions. The Descriptor Table determines where the Message Status Word List for each Subaddress or Mode Code is placed in BIU memory.

Interrupt Log List

The BCRTM gives CAPS the option of implementing an interrupt driven interface. CAPS does not implement an interrupt driven interface. If implemented, this area of memory is set aside to store information about each interrupt occurrence. A minimum length interrupt log list has been created even though interrupts are not used.

Phantom RAM

The BCRTM can address 64K of address space. This exceeds the BIU's physical memory space (the first 8K in the above table). CAPS cannot access memory outside the first 8K word block. The Descriptor Table entry for any Subaddress or Mode Code can be configured to cause the BCRTM to access this non-physical memory space when the CDS sends or receives data to/from the indicated Subaddress or Mode Code. The BIU makes use of this address space in the following ways:

1) The Descriptor Table entries for Receive and Transmit Subaddress #3 must be configured to cause the BCRTM to access locations 7E000-7E003h. These addresses are decoded by the BIU ASIC for Discrete Command and Status data. These Descriptor Table entries must be configured this way in all CAPS Descriptor Tables.

2) The Descriptor Table entry for Mode Code 17 must be configured to cause the BCRTM to write to location 77984h. This address is decoded by the BIU ASIC to generate the RTI and DTSTART pulses. This Descriptor Table entry must be set to the same value in all CAPS Descriptor Tables.

CAPS also uses this address space as a place to put unwanted data. Any attempts by the BCRTM to write to this memory space, except as noted above, has no effect on the BIU or BIU memory. Used in this way, the BCRTM address space above the initial 8K words is referred to as “Phantom RAM”. Memory location 7A000h is the JPL recommended location in the Phantom RAM area to send unwanted data. 7A000h is recommended because it takes two bit flips in that address to inadvertently write to BIU memory.

RTI/DTSTART

Messages written to this location of BIU memory generate either the RTI or DTSTART interrupts. Mode code 17 writes to this memory location. The data word 25C3 hex will generate an RTI interrupt. The data word A531 hex will generate a DTSTART interrupt.

Discrete Command/Status

BIU reads from this memory location will return the BIU discrete command bits. BIU writes to this memory location set the CAPS BIU discrete status bits.

4.3.1.3 BIU Interface Board

The BIU hardware interface is located on the BIU interface board. The BIU interface board also contains the hardware interface to the supplemental heater and IMS cover power switches. Table 4.3-7 presents the layout of BIU interface board.

Table 4.3-7 BIUBD Control Memory Map

Register	Address	R/W	Description
BIU Board Status	20000	R	Reading this location provides status information. This data is reported in housekeeping. See Table 4.3-8
BIU Violations	20010	R	Reading this location provides BIU error information. See Table 4.3-9.
BIU Discrete commands	20020	R	Reading this location provides BIU discrete commanding information.
Supplemental Heater On	20000	W	Writing to this location turns on the supplemental heater.
Supplemental Heater Off	20010	W	Writing to this location turns off the supplemental heater
BIU Discrete Status	20040	W	Writing to this location sets the BIU discrete status bits.
Reset BIU	20050	W	Writing to this location resets the BIU.
IMS Cover Power 1 On	20080	W	Write to this location turns on the IMS cover power switch 1.
IMS Cover Power 1 Off	20090	W	Write to this location turns off the IMS cover power switch 1.
IMS Cover Power 2 On	200A0	W	Write to this location turns on the IMS cover power switch 2.
MS Cover Power 2 Off	200B0	W	Write to this location turns off the IMS cover power switch 2.

Table 4.3-8 BIU Status Bit Definitions

Bit	Description	State
15	Not Used	
14	IMS Cover Closed	0 = IMS cover is not closed
		1 = IMS cover is closed
13	Actuator Launch Latch Power 1 Status	0 = Power 1 to ACT launch latch is off
		1 = Power 1 to ACT launch latch is on
12	Actuator Launch Latch Power 1 Status	0 = Power 2 to ACT launch latch is off
		1 = Power 2 to ACT launch latch is on
11	IMS Cover Power 1 Status	0 = Power 1 to IMS cover is off
		1 = Power 1 to IMS cover is on
10	IMS Cover Power 2 Status	0 = Power 2 to IMS cover is off
		1 = Power 2 to IMS cover is on
9	Actuator Power Status	0 = Actuator power is off
		1 = Actuator power is on
8	Supplemental Heater Power Status	0 = Supplemental heater power is off
		1 = Supplemental heater power is on

Table 4.3-9 BIU Violation Bit Definitions

Bit	Description	State
15	Write Protection Violation	0 = No write protection violation
		1 = Write protection violation has occurred
14	BIU Watchdog Timer Expired	0 = Not expired
		1 = Expired

4.3.2 ELS

The ELS subsystem consists of two high voltage generators, amplifiers/discriminators, and a sensor management unit (SMU). The SMU is built around two ASICs containing counters, latches, high voltage generator control, timing circuitry, and test pulser. A simplified block schematic is shown in Figure 4.3-1.

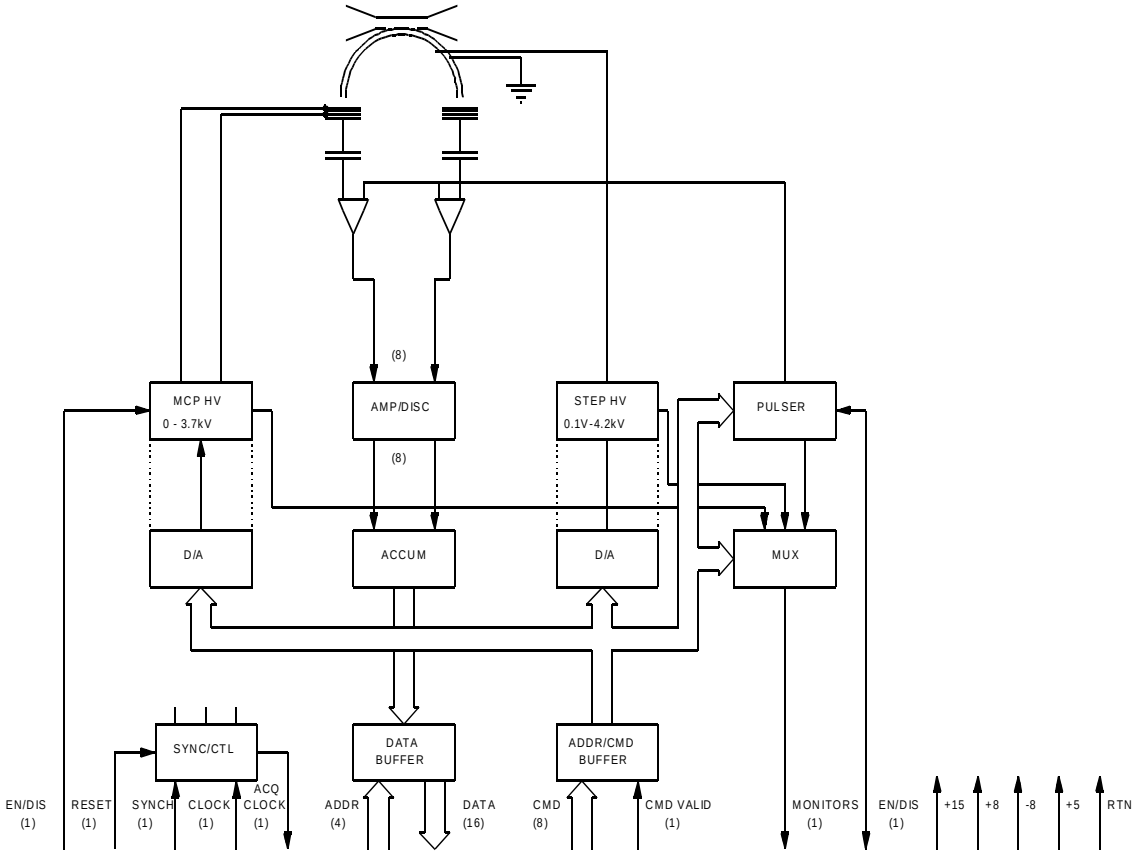


Figure 4.3-1 Simplified ELS Block Diagram.

The interface is provided through the IBS/ELS interface board. ELS shares memory space with IBS. The registers relevant to ELS are shown in Table 4.3-10.

Table 4.3-10 ELS Memory Map

Register	Address (hex)	R/W	Description
Load Sample Clock Rate	30000	W	This register is used to set the sample clock rate by writing a 0, 1 or 2
Set Sample Clock Rate	30010	W	Writing to this register clocks the sample clock rate in
Start/Restart Sample Timing.	30020	W	Writing to this register arms a hardware latch that will begin the system timing (7.8125 msec clock) at the next RTI.
ELS Data	30030-30037	R	These registers contain the eight E/Q ELS data samples
ELS Status	30038-3003B	R	These four registers contain ELS status information. This information is reported in housekeeping.
ARM_SYNC	30030	W	Writing to this register sets a latch to synchronize the sample clock to the RTI pulse.
Read IBS/ELS Status	30040	R	This register contains the ELS and IBS hardware status.
Write ELS	30040	W	This register is the command interface to ELS.
CLR_IBEL_STAT-	30050	W	Writing to this register clears the IBS/ELS status register.
ELS_PWR_ON-	30080	W	Writing to this register turns on ELS power
ELS_PWR_OFF-	30090	W	Writing to this register turns off ELS power

Table 4.3-11 IBS/ELS Status Register Bit Definitions

Bit	Description	State
15	IBS Power Status	0 = IBS Power Off
		1 = IBS Power On
14	ELS Power Status	0 = ELS Power Off
		1 = ELS Power On
13	ELS Sample	A “1” in this bit indicates the ELS sensor is in its dead time period. ELS data can be retrieved during the dead time period.
12	IBS Sample Clock	A “1” in this bit indicates the IBS sensor is in its dead time period. IBS data can be retrieved during the dead time.
11	IMS Integrate	A “1” in this bit indicates the IMS sensor is in its dead time period.
10	SMU Sync	ELS Sensor Management Unit sync pulse. A “0” in this bit indicates the start of a sweep period.
9	TIM_Stat1	Sample clock multiplier bit 1
8	TIM Stat0	Sample clock multiplier bit 0
7	ACT Sync	The actuator sync pulse.

Table 4.3-12 ELS Command Definitions

CMD Addr	CMD Bits	Command	CMD at PWR-UP	Destination
0	4 - 0	Not Used.	-	
1	4	Deadtime Control 0 = 1/8 Deadtime 1 = 2/8 Deadtime	0	SMU
	3 - 0	Not Used.	-	
2	4 - 0	MCP High Voltage Control, 5 LSB's	0	Sensor
3	4	Not Used	-	
	3	Sweep Disable/Enable Control 0 = Sweep Disable (Mode A) 1 = Sweep Enable (Mode B-E)	0	SMU
	2	Sweep Length Control 0 = 1 Step (Mode A) 0 = 32 Steps (Mode C-E) 1 = 64 Steps (Mode B)	0	SMU
	1 - 0	Sweep dE/E Control 0 = 16 % (Mode A & C0) 1 = 16 % (Mode A & C1) 2 = 25 % (Mode A & D) 3 = 36 % (Mode A & E)	3	SMU
4	4 - 0	Sweep Preset Control (Mode A & C0)	31	SMU
5	4	Grid Control 0 = Grid Disable 1 = Grid Enable	0	SMU
	3	Not Used	-	
	2 - 0	Monitor Channel Select Control 0 = +15V Monitor 1 = Sweep HV Monitor 2 = MCP HV Monitor 3 = MCP Current Monitor 4 = MCP Temperature Monitor 5 = HV Enable/Disable Monitor 6 = Not used 7 = Stim Amplitude Monitor	0	SMU

6	4 - 3	Not Used	-	
	2	MCP High Voltage Control, MSB	0	Sensor
	1	Sweep HV On/Off Control 0 = Off 1 = On	0	Sensor
	0	MCP HV On/Off Control 0 = Off 1 = On	0	Sensor
7	4 - 2	Stim. Generator Amplitude Control 0 = 25 mV	0	SMU
	1	1 = 30 mV 2 = 35 mV 3 = 40 mV 4 = 45 mV	0	SMU
	0	5 = 50 mV 6 = 55 mV 7 = 120 mV	0	SMU
		Stim. Generator Mode 0 = Constant 1 = Variable		
		Stim. Generator Enable/Disable 0 = Disable 1 = Enable		

Note: 1. A command is an 8 bit binary pattern where
CMD Addr = 3 MSB where bit 7 = MSB and bit 5 = LSB
CMD Bits = 5 LSB where bit 4 = MSB and bit 0 = LSB
2. A Sweep Command requires that both Addr 3 and Addr 4 commands are updated. Addr 3 must be updated before Addr 4.
3. MCP High Voltage Command requires that both address 2 and address 6 commands are updated. This must happen within 100 µs.

4.3.2.1 MCP High Voltage Power Supply

The MCP power supply provides the bias voltage for the microchannel-plates. It is under control of CPU1 and is 6-bit programmable. See 5548-ELS for a table of the MCP High Voltage control values.

4.3.2.2 Stepping Power Supply

The stepping power supply controls the deflection voltage to the electrostatic analyzer. It steps through 63 logarithmically spaced voltage steps (plus one flyback step). The voltage range is 0.1 to 4200 volts. The high voltage step tables are stored in the SMU. Three sweep tables with different energy step spacing are available. The table selection is controlled by the DPU.

Sweep Table 1 contains 64 values and controls the power generator in 16 % decrements. 64 or 32 values sweeps can be selected from this table. In 32 value sweeps, 32 values of the 64 available can be selected by setting the starting point of the energy sweep to any address value between 0 and 32. The 64 and 32 value sweeps and the starting point in the table is controlled by the CPU1. Sweep Table 2 contains 32 values with 25 % decrements. All values in this table are used in each energy sweep. Sweep Table 3 contains 32 values with 36 % decrements. All values in this table are used in each energy sweep. The sweep table arrangement in the SMU ROM is shown in Figure 4.3-2.

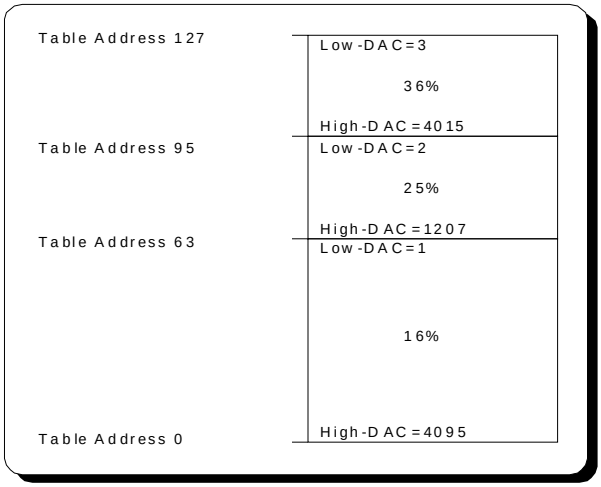


Figure 4.3-2 High Voltage Step Tables

4.3.2.3 ELS Data

CPU 1 reads ELS data by addressing the data latches in the SMU. Four data address lines are be provided making it possible to access the sixteen data latches. The data latches should not be read during the first 10 µs of the accumulation dead-time since the latches are updated during this period. The data from the previous accumulation period are available during the current accumulation period and can be read at any time during the current accumulation period. Eight data counters plus four status registers are available to be read. The CPU1 issues commands to the ELS sensor over a one way, 8 bit command interface. The three MSB's of the command word define the type of command, and the five LSB's contain the command data. See Tables 4.3-4 and 4.3-5.

Table 4.3-13 ELS Counter-data Allocation

Address	Counter Channel
0	Counter Channel 0
1	Counter Channel 1
2	Counter Channel 2
3	Counter Channel 3
4	Counter Channel 4
5	Counter Channel 5
6	Counter Channel 6
7	Counter Channel 7

Table 4.3-14 ELS Status Data Allocation

Address	Status Bits	Status
8	Command Status	
	Bit 0 = MCP HV Disable/Enable Control	CST
	Bit 1 = Sweep HV Disable/Enable Control	CST
	Bit 2 = MCP Bit 5 (MSB)	CST
	Bit 3 = x (x = don't care)	
	Bit 4 = x	
	Bit 5 = Analog Monitor Address 0 (LSB)	CST
	Bit 6 = Analog Monitor Address 1	CST
	Bit 7 = Analog Monitor Address 2	CST
	Bit 8 = x	
	Bit 9 = Grid Disable/Enable Control	CST
9	Command Status	
	Bit 0 = Sweep Preset Disable/Enable	FST
	Bit 1 = Sweep 32/64 Step	CST
	Bit 2 = Sweep Disable/Enable	CST
	Bit 3 = Sweep Preset Bit 0 (LSB)	CST
	Bit 4 = Sweep Preset Bit 1	CST
	Bit 5 = Sweep Preset Bit 2	CST
	Bit 6 = Sweep Preset Bit 3	CST
	Bit 7 = Sweep Preset Bit 4	CST
	Bit 8 = dE/E Control Bit 0 (LSB)	CST
	Bit 9 = dE/E Control Bit 1	CST
10	Command Status	
	Bit 0 = MCP Bit 0 (LSB)	CST
	Bit 1 = MCP Bit 1	CST
	Bit 2 = MCP Bit 2	CST
	Bit 3 = MCP Bit 3	CST
	Bit 4 = MCP Bit 4	CST
	Bit 5 = Stim Disable/Enable	CST
	Bit 6 = Stim Mode	CST

	Bit 7 = Stim Amplitude Bit 0 (LSB) Bit 8 = Stim Amplitude Bit 1 Bit 9 = Stim Amplitude Bit 2	CST CST CST
11	Command Status Bit 0 = Sample Number Bit 0 (LSB) Bit 1 = Sample Number Bit 1 Bit 2 = Sample Number Bit 2 Bit 3 = Sample Number Bit 3 Bit 4 = Sample Number Bit 4 Bit 5 = Sample Number Bit 5 Bit 6 = Deadtime Short/Long Bit 7 = Stim Amplitude Bit 0 (LSB) Bit 8 = Stim Amplitude Bit 1 Bit 9 = Stim Amplitude Bit 2	 FST FST FST FST FST FST FST FST FST FST

Status Codes are: CST = Command Status FST = Functional Status

4.3.2.4 Analog Data

The ELS generates a single multiplexed analog signal containing all sensor housekeeping data. The analog data present on the interface is determined by commands sent to the ELS over the 8 bit command interface. The delay from receipt of command to delivery of stable analog data is less than 500 μs. Analog data is digitized with 12 bits resolution. See section 5.3.3.4.2, Monitor Data Acquisition, for more information.

4.3.3 IBS

The IBS subsystem consists of two high voltage power supplies, 3 pre-amplifiers, power supply control DAC's, and test pulser. A simplified block schematic is shown in Figure 4.3-3. Table 4.3-15 presents the IBS command memory layout.

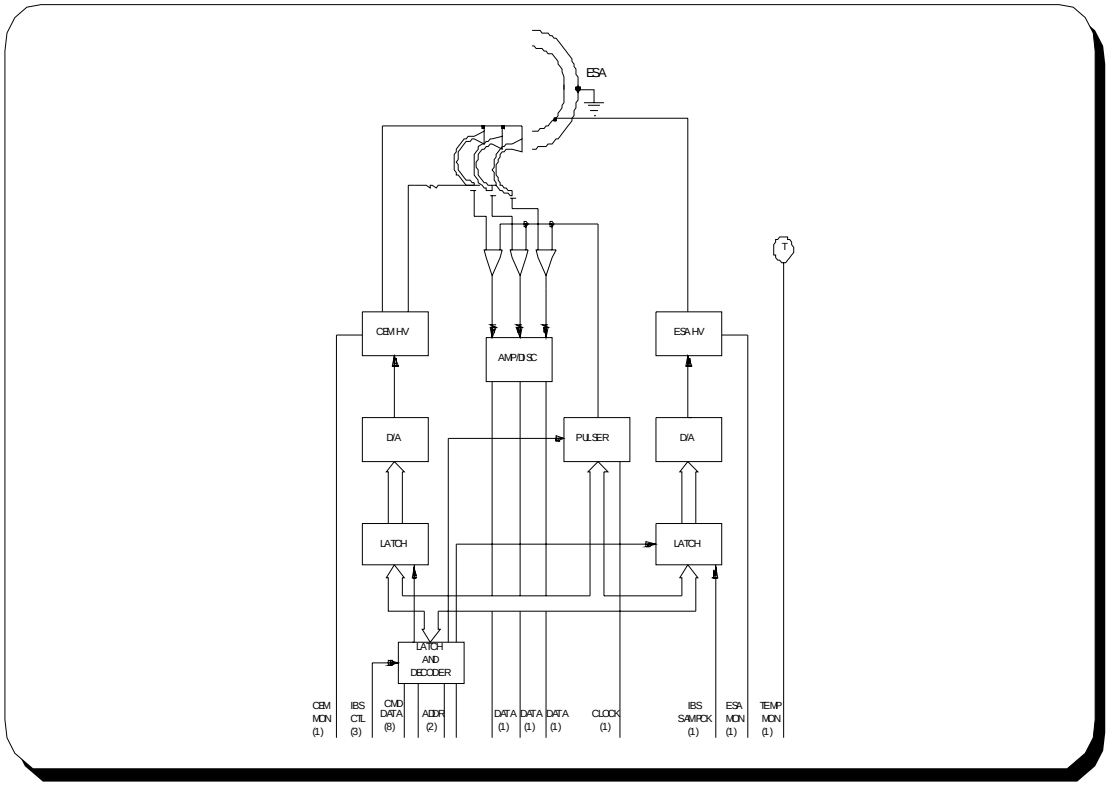


Figure 4.3-3 Simplified IBS Block Diagram.

Table 4.3-15 IBS Command Memory Map

Register	Address	R/W	Description
ESA Voltage Control LSB	28000h	R/W	This register contains the low order eight bits of the ESA voltage DAC. This occupies bits 8-15.
ESA Voltage Control MSB High Voltage Enable/Disable Status High Voltage Safe/Arm Status	28001h	R/W	This register contains the high order six bits of the ESA voltage DAC, high voltage control status and high voltage state status. The ESA DAC occupies bits 10-15. The high voltage control status bit occupies bit 8 and the high voltage state status bit occupies bit 9.
CEM Voltage Control	28002h	R/W	This register contains the CEM voltage control DAC. The CEM voltage control DAC occupies bits 8-15.
Stim Control	28003h	R/W	This register contains the IBS STIM control register. The register is divided into three functions: Channel Select – Bits 8-10 On/Off – Bit 11 Control – Bits 12-15

Table 4.3-16 presents the memory map for the IBS/ELS Control Board relevant to IBS.

Table 4.3-16 IBELSBD IBS Control Memory Map

Register	Address	R/W	Description
Counter 1	30000	R	IBS channel 1 counter
Counter 2	30010	R	IBS channel 2 counter
Counter 3	30020	R	IBS channel 3 counter
IBS/ELS Status	30040	R	IBS/ELS board status register. See Table 4.3-11.
Clear IBS/ELS status	30050	W	Writing to this register clears the IBS/ELS board status register.
IBS Power On	300A0	W	Writing to this register turns on IBS high voltage power.
IBS Power Off	300B0	W	Writing to this register turns off IBS high voltage power.
Arm IBS	300C0	W	Writing to this register arms the IBS high voltage.
Safe IBS	300D0	W	Writing to this register safes the IBS high voltage.
Enable IBS	300E0	W	Writing to this register enables the IBS high voltage.
Disable IBS	300F0	W	Writing to this register disables the IBS high voltage

4.3.3.1 CEM Power Supply

The CEM power supply provides the negative bias voltage for the three channel electron multipliers. It is controlled by CPU1 and is 8-bit programmable from 0 to -4.0 kV. The CEM voltage is set by writing an eight bit word to the CEM DAC register. The register is located at address Base+2. Updating can take place at any instant and will take immediate effect. The current contents of the CEM DAC register can be read at address Base+2.

4.3.3.2 ESA Power Supply

The ESA power supply provides the negative deflection voltage to the electrostatic analyzer. IBS is designed to operate at voltage stepping (sampling) rates that are up to eight times faster than those of ELS and IMS. The nominal IBS ESA stepping period is 7.8125 ms. IBS stepping will be controlled by tables of step numbers stored in the CPU1 memory.

The ESA supply covers the voltage range from -2600 V to -0.05 V in 1.27% increments giving 852 voltage levels. In order to have sufficient resolution over the full range, the power supply is designed as a three range supply with each range being controlled by a 12 bit DAC. The ESA voltage is commanded to the desired level by updating the 14-bit ESA buffer register. This is done by writing the eight LSB's to the ESA buffer register at address Base+0 and the four MSB's plus the two range bits to the ESA buffer register at address BASE+1. This updating can occur at any instant during the IBS data acquisition time. The update will not take immediate effect but is transferred to the ESA DAC register at the beginning of the following dead time. The current contents of the ESA DAC register can be read by the CPU1 at addresses Base+0 (LSB's) and Base+1 (MSB's and range bits).

4.3.3.3 IBS Data

The IBS data is passed from the Pre-Amplifier-Discriminators (PAD's) to the DPU over 3 pairs of wire. The signal wires are connected to counters located in the DPU. The counters are read and reset by the CPU1 after each accumulation period.

4.3.3.4 IBS Stim Pulse Generator

The DPU generates a stim pulse to be used for testing the IBS. The frequency is 1.048576 MHz. The stim function is controlled by writing an eight bit control word to the stim register at address Base+3. The control word has the following functions:

Select stim pulse frequency.

The frequency can be 1.048576 MHz divided by 2 through 16. The ratio is selected by loading the stim register bits 12 - 15 (Bit 15 = LSB) with a value of 16 minus the desired ratio. Table 4.3-17 shows the stim frequencies.

Table 4.3-17 IBS Stim Frequencies

Contr. Bits 12-15	Stim Frequency	Contr. Bits 12-15	Stim Frequency
0H	65.536 kHz	8H	131.072 kHz
1H	69.905 kHz	9H	149.797 kHz
2H	74.898 kHz	AH	174.763 kHz
3H	80.660 kHz	BH	209.715 kHz
4H	87.381 kHz	CH	262.144 kHz
5H	95.325 kHz	DH	349.525 kHz
6H	104.858 kHz	EH	524.288 kHz
7H	116.508 kHz	FH	Illegal, No Stim

Switch on stim.

A logic “1” in stim register bit 11 will activate stim.

Select channel.

Stim register bits 8, 9 and 10 (Bit 8 = MSB) control the channels to be exercised. Any or all 3 channels can be selected by loading a “1” in the appropriate register bit location.

4.3.3.5 IBS Acquisition Clock

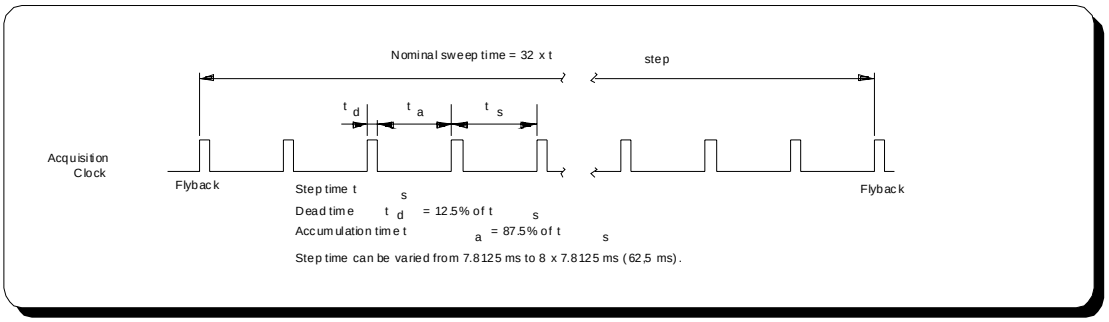


Figure 4.3-4 IBS Acquisition Clock

4.3.3.6 IBS Monitors

The IBS generates 3 analog signals representing two high voltage monitors and the IBS temperature. Analog data is digitized to a precision of 12 bits. The input signal ranges 0.0 to 5.0 volts for the analog signal. See section 5.3.3.4.2, Monitor Data Acquisition, for more information.

4.3.4 High Voltage Unit Control Board

The High Voltage Unit Control board provides the interface to high voltage supplies HVU-1 and HVU-2. It also provides the analog-to-digital converter for monitor acquisition. Table 4.3-18 presents the memory map for the High Voltage Unit Control Board.

Table 4.3-18 HVUBD Memory Map

Register	Address	R/W	Description
ADC Value	40000	R	Reading this location provides the last value converted by the ADC.
Arm HVU-1	40000	W	Writing any value to this location arms HVU-1.
Read HVU Status	40004	R	Reading this location provides the HVU status. See Table 4.3-11.
Safe HVU-1	40004	W	Writing any value to this location safes HVU-1.
Enable HVU-1	40008	W	Writing any value to this location enables HVU-1.
Disable HVU-1	4000C	W	Writing any value to this location disables HVU-1.
Arm HVU-2	40010	W	Writing any value to this location arms HVU-2.
Safe HVU-2	40014	W	Writing any value to this location safes HVU-2.
Enable HVU-2	40018	W	Writing any value to this location enables HVU-2.
Disable HVU-2	4001C	W	Writing any value to this location disables HVU-2.
Set MUX	40020	W	CAPS has a single A/D converter. Writing to this register selects a signal to be converted.
Accelerate Voltage	40028	W	Writing a value to this registers sets the accelerate DAC.
Retard Voltage	4002C	W	Writing a value to this register sets the retard voltage

Register	Address	R/W	Description
HVU-1 Power On	40030	W	Writing any value to this location turns power on to HVU-1. There are two power switches for HVU-1 writing a 1 to this location turns on switch 1. Writing a 2 to this locations turns on switch 2.
HVU-1 Power Off	40034	W	Writing any value to this location turns power off to HVU-1.
HVU-2 Power On	40038	W	Writing any value to this location turns power on to HVU-2.
HVU-2 Power Off	4003C	W	Writing any value to this location turns power off to HVU-2.

Table 4.3-19 HVU Status Bit Definitions

Bit	Description	States
15	Analog-to-Digital Converter Status	0 – Not Converted
		1 – Conversion Complete
14	HVU-1 Power Switch 1 Status	0 – Off
		1 – On
13	HVU-1 Power Switch 2 Status	0 – Off
		1 – On
12	HVU-2 Power Status	0 –Off
		1 On
11	HVU-1 State Status	0 – Safed
		1 – Armed
10	HVU-1 Control Status	0 – Disabled
		1 – Enabled
9	HVU-2 State Status	0 – Safed
		1 – Armed
8	HVU-2 Control Status	0 – Disabled
		1 – Enabled

4.3.5 High Voltage Unit #1

The ±16 kV high voltage power supply provides a dual polarity DC high voltage output adjustable in the range from ±8 kV to ±16 kV for the IMS. The negative and positive high voltages provide a balanced high voltage across the Linear Electric Field (LEF) resistor divider stack to produce a tuned linear electric field within the IMS. The negative high voltage power supply also provides a floating 1200 volts for the LEF microchannel plate (see 5548-IMS for details).

The positive and negative high voltage outputs are provided by separate power supplies such that they have separate control and monitor lines. This will provide redundancy such that if the positive power supply were to fail, it could be turned off without interfering with the negative power supply. (The IMS can operate in a degraded mode with the negative supply only.)

Table 4.3-20 lists the individual HVU-1 power supplies and a simplified block diagram is shown in Figure 4.3-5.

Table 4.3-20 High Voltage Power Supplies in HVU-1

Subsystem	Requirements	Comments
Retard High Voltage	+16 kV programmable from 0 V to +16 kV	8 Bit Resolution
Accel. High Voltage	-16 kV programmable from 0 V to -16 kV	8 Bit Resolution
Floating LEF MCP HV	1.2 kV when Acc. HV is between -10.7 and -16 kV	Fixed

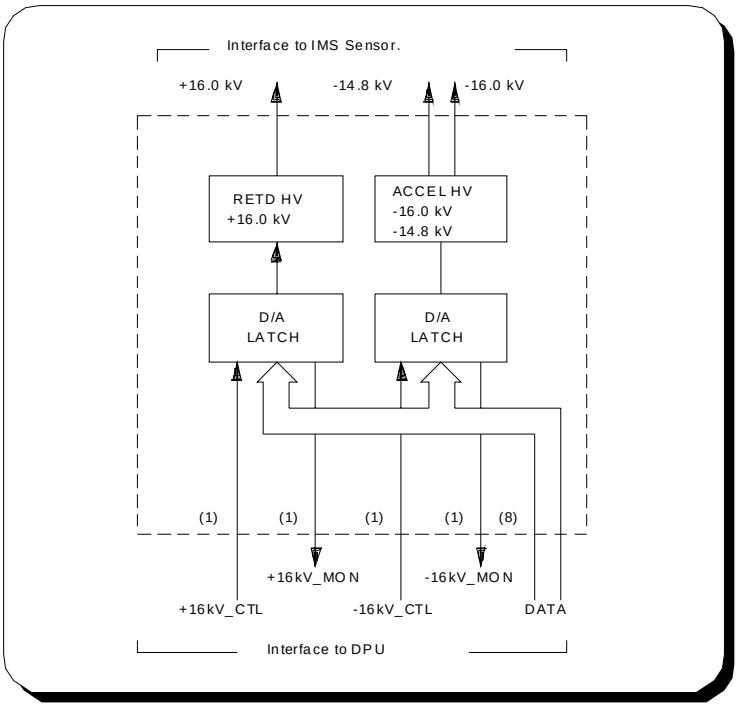


Figure 4.3-5 Simplified HVU-1 Block Diagram

4.3.5.1 Retarding High Voltage Power Supply (RHVPS)

The RHVPS provides the positive retarding voltage for the LEF section of the IMS. It is programmable from 0 V to +16 kV. The RHVPS is operating within specifications when the output voltage is between +8 kV and +16 kV.

4.3.5.2 Accelerating High Voltage Power Supply (AHVPS)

AHVPS provides the negative accelerating voltage for the LEF section of the IMS. It is programmable from 0 V to -16 kV. The AHVPS operates within specifications when the output voltage is between -8 kV and -16 kV. The AHVPS also provides the power required to operate the Floating LEF MCP HVPS.

4.3.5.3 Floating LEF MCP High Voltage Power Supply

The Floating LEF MCP High Voltage Power Supply provides +1200 VDC relative to the AHVPS output when the AHVPS output is between -10.7 kV and -16 kV. When the AHVPS is at its maximum output voltage of -16 kV, the output of the Floating LEF MCP HVPS is -14.80 kV relative to ground potential. The bias voltage for the floating LEF MCP is fixed and cannot be varied. CPU1 has no control functions relating to the Floating LEF MCP HVPS.

4.3.5.4 Analog Data (±16KV_MON)

Each high voltage power supply generates an analog signal representing a high voltage monitor. Analog data will be digitized to a precision of 12 bits. See section 5.3.3.4.2, Monitor Data Acquisition, for more information.

4.3.6 High Voltage Unit #2 (HVU-2)

The HVU-2 provides the high voltages needed by the microchannel plates and the electrostatic analyzer in the IMS. It consists of three high voltage power supplies. The high voltage power supplies are designed to be free of corona and are short circuit protected.

A simplified block diagram is shown in Figure 4.3-6 and Table 4.3-21 lists the individual power supplies.

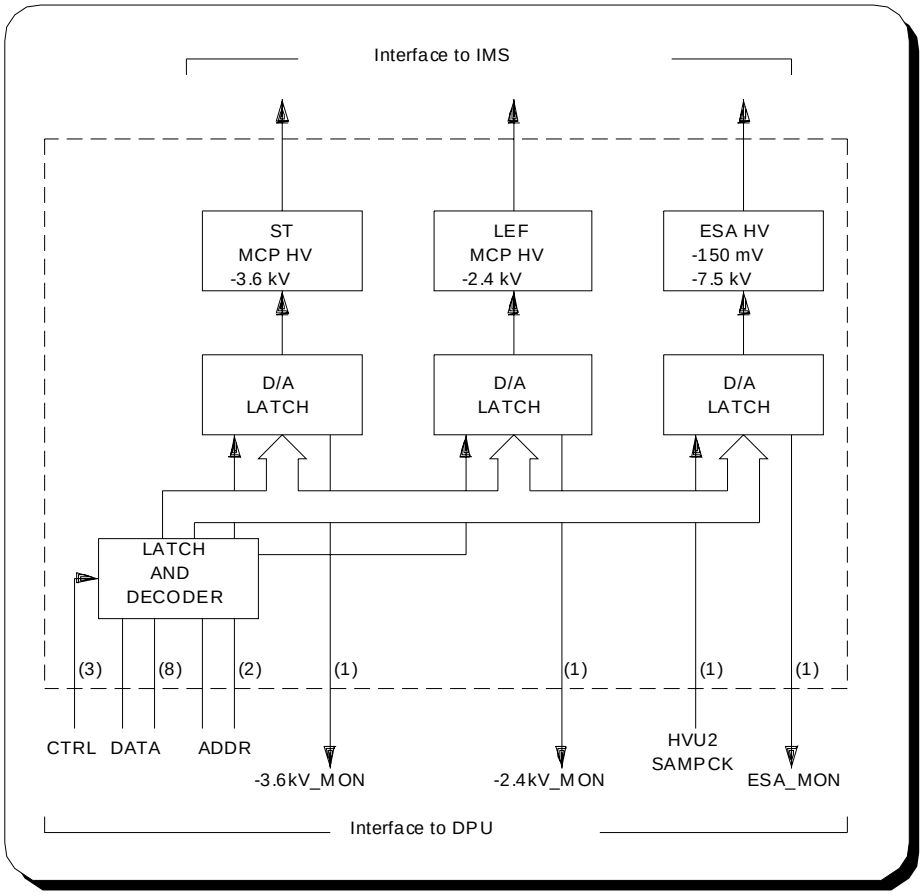


Figure 4.3-6 Simplified HVU-2 Block Diagram.

Table 4.3-21 HVU-2 High Voltage Power Supplies

Subsystem	Requirements	Comments
ST MCP High Voltage	-3.6 kV programmable from -.5 kV to -3.6 kV	8 Bit Resolution
LEF MCP High Voltage	-2.4 kV programmable from -.5 kV to -2.4 kV	8 Bit Resolution
ESA Step Supply	-7.415 kV programmable from -.16 V to -7.415 kV	12 Bit Resolution 3 Ranges

4.3.6.1 ST MCP High Voltage Power Supply

The ST MCP High Voltage Power Supply provides the bias voltage for the ST MCP. It is under control of the DPU and is 8-bit programmable from -0.5 kV to -3.6 kV. The supply is powered from the +15 volts generated by the low voltage power supply in the DPU. The +15 volt line is controlled by a solid state switch in the DPU.

4.3.6.2 LEF MCP High Voltage Power Supply

The LEF MCP High Voltage Power Supply provides the bias voltage for the second and third stages of the LEF MCP. It is under control of the DPU and is 8-bit programmable from -0.5 kV to -2.4 kV. The supply is powered from the +15 volts generated by the low voltage power supply in the DPU. The +15 volt line is controlled by a solid state switch in the DPU.

4.3.6.3 ESA Step Power Supply

The ESA Step Power Supply provides the deflection voltage for the IMS electrostatic analyzer section of the IMS. During an energy sweep it steps through 63 logarithmically spaced voltage levels (plus one flyback step). Steps are selected from a table of 63 levels by command from the DPU. The voltage range is -0.16 V to -7415 V. Table 4.3-22 Lists the HVU-2 Stepping Supply Ranges.

Table 4.3-22 HVU-2 Stepping Supply Ranges

Range	Step No.	Multiplier	D/A Numeric Value	Voltage
HIGH RANGE	0	1.810745	4095	7415.000
	20		128	231.7139
MED RANGE	21	0.04758171	4095	194.8471
	41		128	6.0888
LOW RANGE	42	0.00125033	4095	5.1201
	62		128	0.160

4.3.6.4 ESA Voltage Control

The ESA voltage is commanded to the desired level by updating the 14-bit ESA buffer register. This is done by writing the eight LSB's to the ESA buffer register at address Base+0 and the four MSB's plus the two range bits to the ESA buffer register at address BASE+1. This updating can occur at any instant during the IMS data acquisition time. The update does not take immediate effect but will be transferred to the ESA DAC register at the beginning of the following dead time. The current contents of the ESA DAC register can be read by the DPU at addresses Base+0 (LSB's) and Base+1 (MSB's and range bits).

4.3.6.5 LEF MCP High Voltage Control

The LEF MCP voltage is set by writing an eight bit word to the LEF MCP DAC register. The register is located at address Base+2. Updating can take place at any instant and will take immediate effect. The current contents of the LEF MCP DAC register can be read at address Base+2.

4.3.6.6 ST MCP High Voltage Control

The ST MCP voltage is set by writing an eight bit word to the ST MCP DAC register. The register is located at address Base+3. Updating can take place at any instant and will take immediate effect. The current contents of the ST MCP DAC register can be read at address Base+3.

4.3.6.7 HVU-2 Sample Clock (HVU2_SAMPCK-)

The ESA power supply stepping is uniquely controlled by the DPU, and synchronized to the IMS data acquisition. The timing is shown in Figure 3.1.3.7. The basic CAPS step time is 62.5 ms, an can be expanded up to 8 x 62.5 ms (500 ms).

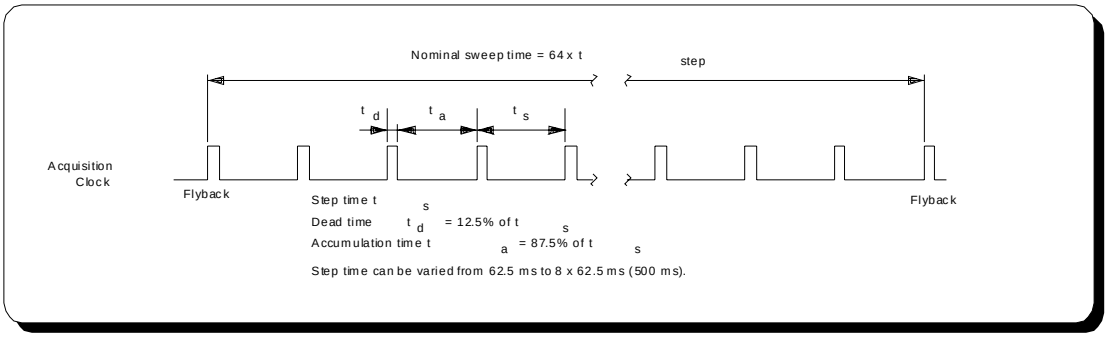


Figure 4.3-7 HVU-2 Sample Clock.

4.3.6.8 Analog Data

Each high voltage power supply generates an analog signal representing high voltage monitors, and one HVU-2 temperature monitor is provided. Analog data is digitized to a precision of 12 bits. The input signal range shall be 0.0 to 5.0 volts for the analog signal. See section 5.3.3.4.2, Monitor Data Acquisition, for more information.

4.3.7 Actuator

The primary function of the ACT is to provide articulation for the entire CAPS instrument over a range of ±104° in a windshield-wiper mode of operation. The nominal scan range is ±92° with 12° at either end for acceleration and deceleration. Note, due to anomaly during ICO 1, it is not recommended CAPS be actuated beyond -80°. The ACT consists of the following elements:

a) motor and associated drive electronics
b) bearings
c) position encoder, end-position indicators (2) and associated electronics
d) launch “latch” and a means of taking up launch loads from bearings
e) Wax Thermal Actuator (WTA) used to release launch latch
f) flexible “cable wrap” from S/C interface to DPU interface
g) mechanical structure to house all of the above and interface to S/C
h) purge line connection between CAPS and S/C
i) MLI brackets

The ACT encoder provides a continuous position readout accurate to ±0.5°. There is also be an additional means of reading out ACT position at the two extremes of motion (at the hard stops at ±108°) by means of two limit switches. The CPU 1 transmits two 8-bit command words to the ACT control electronics (ACT Base Address+0 and ACT Base Address+1) at a fixed rate of one set of commands per 7.81250 milliseconds to control acceleration, scan, deceleration

and stop modes of the ACT. The two ACT command words can be transferred from the DPU at any instant between the ACT_SYNC- pulses and will take effect at the rising edge of the following ACT_SYNC- pulse.

The ACT provides an 8-bit register to allow the DPU to read status information (Limit Switches) from the ACT. A position potentiometer, located in ACT, shall provide an analog voltage indicating the angular position of the ACT. The actuator interfaces is part of the BIU interface board. Table 4.3-23 presents the actuator memory layout relevant to the actuator.

Table 4.3-23 BIUBD Control Memory Map

Register	Address	R/W	Description
Actuator Hard Limits	20060	R	Reading this location provides the status of the actuator limit switches.
Actuator Power On	20020	W	Writing to this location turns on the actuator 20V supply.
Actuator Power Off	20030	W	Writing to this location turns off the actuator 20V supply.
Actuator X	20060	W	Writing to this location sets the actuator position X component
Actuator Y	20061	W	Writing to this location sets the actuator position Y component
Actuator Feedback	20062	R	Reading this location provides actuator wobble compensation feed back.
Actuator Launch Latch Power 1 On	200C0	W	Write to this location turns on the actuator launch latch power switch 1.
Actuator Launch Latch Power 1 Off	200D0	W	Write to this location turns off the actuator launch latch power switch 1.
Actuator Launch Latch Power 2On	200E0	W	Write to this location turns on the actuator launch latch power switch 2.
Actuator Launch Latch Power 2 Off	200F0	W	Write to this location turns off the actuator launch latch power switch 2.

Table 4.3-24 BIU Status Bit Definitions

Bit	**Description**	**State**
13	Actuator Launch Latch Power 1 Status	0 = Power 1 to ACT launch latch is off
		1 = Power 1 to ACT launch latch is on
12	Actuator Launch Latch Power 1 Status	0 = Power 2 to ACT launch latch is off
		1 = Power 2 to ACT launch latch is on
10	IMS Cover Power 2 Status	0 = Power 2 to IMS cover is off
		1 = Power 2 to IMS cover is on
9	Actuator Power Status	0 = Actuator power is off
		1 = Actuator power is on

Table 4.3-25 Actuator Limit Bit Definition

Bit	Description	State
0	HARD LIMIT 1	0 = Hard limit 1 not reached 1 = Hard limit 1 reached
1	HARD LIMIT 2	0 = Hard limit 2 not reached 1 = Hard limit 2 reached

4.3.7.1 Launch Latch

The ACT_LATCH command (see section 5.8.1.1) releases the actuator launch latch by activating a TWA (Thermal Wax Actuator). This command contains two parameters to turn on/off the two launch latch power circuits. The primary power circuit contains a feedback circuit (microswitch) that will turn the primary power off after latch release. If the primary power fails to release the launch latch it must be turned off manually. If primary power fails to activate the latch, the secondary power circuit can be activated with this command. This circuit has no feedback, therefore it must be turned off manually (again using this command). If the secondary power circuit also fails to activate the TWA, then both the primary and secondary circuits can be turned on together. The primary power will be turned off by the activation of the TWA but the secondary power must be turned off by command. If using both power controls fail to activate the TWA then both power circuits must be turned off by command.

NOTE: The TWA was successfully released during ICO 1. The above discussion remains for historical purposes.

4.3.7.2 Movement

If the actuator is enabled, the transition to the new FOV is accomplished using the following algorithm:

```
Read the actuator position feedback 3 times and compute the average feedback
If the actuator is running then
  if TEMP_ACCEL = 0 then
    WOBBLE_OFFSET := WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(FAST_DECEL);

  elsif TEMP_ACCEL = 1 then
    WOBBLE_OFFSET := WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(SLOW_DECEL);

  elsif TEMP_ACCEL <= 3 then
    WOBBLE_OFFSET := WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(NO_ACCEL);

  elsif TEMP_ACCEL <= 7 then
    WOBBLE_OFFSET := WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(SLOW_ACCEL);

  elsif TEMP_ACCEL <= 15 then
    WOBBLE_OFFSET := WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(FAST_ACCEL);
  end if;

else
  -- must be accelerating or decelarating
  -- use a different compensation table
  if TEMP_ACCEL = 0 then
    WOBBLE_OFFSET := AD_WOBL_TABLE ACTUATOR_POSITION_OFFSET)(FAST_DECEL);

  elsif TEMP_ACCEL <= 1 then
    WOBBLE_OFFSET := AD_WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(SLOW_DECEL);

  elsif TEMP_ACCEL <= 3 then
    WOBBLE_OFFSET := AD_WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(NO_ACCEL);

  elsif TEMP_ACCEL <= 7 then
    WOBBLE_OFFSET := AD_WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(SLOW_ACCEL);

  elsif TEMP_ACCEL <= 15 then
    WOBBLE_OFFSET := AD_WOBL_TABLE (ACTUATOR_POSITION_OFFSET)(FAST_ACCEL);
 end if;
end if;
PHASE_POINTER := PHASE_POINTER + LONG_INTEGER(WOBBLE_OFFSET);
```

See Appendix M for a listing of the actuator data and wobble compensation values. The minimum FOV is 28 degrees and the maximum FOV is ±100 . The FOV is defined in units of 4 , i.e., ±28 , ±32 , ±36 , etc. The FOV limits are constraint checked by the ground system and are not constraint checked by the flight software.

The mode parameter determines the movement of the actuator. The FOV mode uses the Limit 1 and Limit 2 parameters to define the length of travel of a "windshield wiper" movement of the actuator. The actuator is accelerated (this requires 12° of movement) from rest to a speed of 1° /sec. This speed is maintained through the FOV and then the actuator is decelerated to rest (again requiring 12° of movement). The 24° of movement required for accelerating and decelerating the actuator are inside the FOV limits.

Note: The actuator cannot and should not be commanded past –80 degrees. If the actuator operates past –85 degrees, the software will automatically switch to the RAM mode, hold the position at –85 degrees and report an error in housekeeping.

The PARK mode moves the actuator to the position given by command parameter Limit 1 and stops (the actuator 20V supply is turned off).

Note: Limit 2 should be set to the same value as Limit 1. The actuator remains in this position until another ACT_FOV and ACT_EXEC command is received.

The RAM mode moves the actuator to a defined position and stops. Command parameters Limit 1 and Limit 2 specify the final position of the actuator. The MAINT mode moves the actuator through a predefined range of movement twice and then stops the actuator at its launch latch position (0°).

4.3.7.3 Temperature Compensation

The temperature compensation algorithm, when enabled by ACT_TEMP_COMP command, adjusts the actuator step table to reduce the power consumption of the actuator. The algorithm is:

```
CurrentActuatorTemperature = -47.9005394 + 0.6271286011 * ActuatorTemperatureMonitor –
0.001936307643 * AactuatorTemperatureMonitor^2 + 1.115957616 E-6 *
ActuatorTemperatureMonitor^3 + 2.579960422 E - 8 * ActuatorTemperatureMonitor^4

Resistance = 86.11 + 0.32485 * Current Actuator Temperature + -1.5062 E –3 *
Current Actuator Temperature^2

Scale Factor = Square Root (120.0 / 1000.0) * Resistance / 13.485)

For all the actuator step data loop
  Actuator Data[index].PhaseA = (127 – (127 – ActuatorData[Index].PhaseA and
  0x7F) * Scale Factor *0.5) + (ActuatorData[index].PhaseA and 0x80)

  Actuator Data[index].PhaseB = (127 – (127 – ActuatorData[Index].PhaseB and
  0x7F) * Scale Factor *0.5) + (ActuatorData[index].PhaseB and 0x80)
End loop
```

4.3.7.4 Wobble Compensation

The wobble compensation algorithm, when enabled by the ACT_WOBL_COMP command, attempts to compensate for actuator wobble. The actuator should move at a constant 1°/second rate. The wobble compensation algorithm is:

```
Read the actuator feedback register three times and compute the average value

If the actuator is running at 1°/second then

 If the feedback was 0 then
   Get the wobble compensation index from the wobble compensation table for
   fast deceleration
 Else if the feedback was 1 then
   Get the wobble compensation index from the wobble compensation table for
```

```
   slow deceleration
 Else if the feedback was or less 3 then
   Get the wobble compensation index from the wobble compensation table for no
   acceleration
 Else if the feedback was or less 7 then
   Get the wobble compensation index from the wobble compensation table for
   slow acceleration
 Else if the feedback was or less 15 then
   Get the wobble compensation index from the wobble compensation table for
   fast acceleration

Else

 If the feedback was 0 then
   Get the wobble compensation index from the acceleration/deceleration wobble
   compensation table for fast deceleration
 Else if the feedback was 1 then
   Get the wobble compensation index from the acceleration/deceleration wobble
   compensation table for slow deceleration
 Else if the feedback was or less 3 then
   Get the wobble compensation index from the acceleration/deceleration wobble
   compensation table for no acceleration
 Else if the feedback was or less 7 then
   Get the wobble compensation index from the acceleration/deceleration wobble
   compensation table for slow acceleration
 Else if the feedback was or less 15 then
   Get the wobble compensation index from the acceleration/deceleration wobble
   compensation table for fast acceleration

End if

Adjust the actuator step index with the wobble compensation index
```

4.3.8 IMS Cover Latch

The IMS aperture is covered during launch to prevent contamination of the IMS sensor. During early cruise, the IMS cover is released. The IMS cover latch is a TWA similar to the actuator launch latch. The IMS_COVER command is used to release the IMS Cover. This command contains two parameters to turn on/off the two launch latch power circuits. The primary power circuit contains a feedback circuit (microswitch) that will turn the primary power off after latch release. If the primary power fails to release the launch latch it must be turned off manually. If primary power fails to activate the latch, the secondary power circuit can be activated with this command. This circuit has no feedback, therefore it must be turned off manually (again using this command). If the secondary power circuit also fails to activate the TWA, then both the primary and secondary circuits can be turned on together. The primary power will be turned off by the activation of the TWA but the secondary power must be turned off by command. If using both power controls fail to activate the TWA then both power circuits must be turned off by command.

4.3.9 CPU 1 Watchdog

This signal is generated by the CPU 1 PIC watchdog timer. This signal generates a hard reset of the CAPS DPU when the timer expires. The timer is set to expire 32 seconds after the last reset of the CPU 1 PIC watchdog timer. CPU 1 watchdog processing is controlled by the 82CPU1_WATCHDOG command.

4.4 Interrupts Handled by CPU 1

Table 4.3-26 lists the interrupt assignments for CPU 1. The following sections describe the interrupts.

Table 4.3-26 CPU 1 Interrupts

Interrupt	Name	Type
USERINT 0	CPU2_WATCHDOG	Edge Triggered
USERINT 1	ACT_SAMPL_CLK	Edge Triggered
USERINT 2	SPARE	Edge Triggered
USERINT 3	RTI	Edge Triggered
IOINTL 1	SPARE	High Level
USERINT 4	CPU1_IRQ	Edge Triggered
IOINTL 2	SPARE	High Level
USERINT 5	DTSTART (not used by S/W)	Edge Triggered

4.4.1 CPU2_WATCHDOG

The CPU 2 watchdog interrupt is generated by the CPU 2 PIC watchdog timer. This signal indicates a CPU 2 software failure. CPU1 reports the condition in the CPU 1 error bits in housekeeping. CPU 2 watchdog processing is commanded by the 82CPU2_WATCHDOG command.

4.4.2 ACT_SAMPL_CLK

The actuator sample clock interrupt provides the base data acquisition clock timing for CPU1. This signal originates in the timing circuitry located on the IBS/ELS board and is synchronized with the RTI timing signal during CPU1 initialization and is re-synchronized every four seconds with the RTI signal.

4.4.3 DTSTART

The Dead Time Start (DTSTART) interrupt signals the beginning of the dead time period for the 1553B bus communications. This signal is broadcast by the CDS over the bus and is converted to an interrupt to CPU1 by the BIU. This dead time period is guaranteed to be at least 5ms long. This interrupt can occur within a few hundred microseconds after the RTI to 120 milliseconds after the RTI. Because the DTSTART interrupt can occur so shortly after an RTI, the interrupt has been turned off by the CPU 1 PROM and science software and is generated artificially using TIMER A. It is generated 120 milliseconds after the RTI.

4.4.4 RTI

The RTI interrupt signals the beginning of a new bus activity period. This signal is broadcast by the CDS over the bus and is converted to an interrupt to CPU 1 by the BIU. This interrupt is generated every 125 milliseconds. It is the primary clock for generating the instrument telemetry (science data and housekeeping).

4.4.5 CPU1_IRQ

The CPU1 interrupt is used by CPU 2 to notify CPU 1 to process commands from CPU 2. CPU 2 generates this interrupt whenever one or more commands are present in the CPU 1 inter-processor command queue.

4.5 Interrupts Generated by CPU 1

4.5.1 CPU 2 to CPU 1 Command Interrupt

This interrupt is generated by CPU1 when an inter-processor command requires processing by CPU 2. This is generated on a one second boundary (during the dead time of RTI 7).

4.5.2 Artificial DTSTART and RTI Watchdog (Timer A)

The 1750A timer A is used as a watchdog timer for the RTI. Should the RTI not be generated 7 milliseconds after the DTSTART, the timer will expire generating an interrupt. An artificial RTI will be inserted. Following the generation of an RTI interrupt, timer A is set for 120 milliseconds to generate an artificial DTSTART. The DTSTART hardware interrupt is not used.

5 SOFTWARE FUNCTIONAL DESIGN DESCRIPTION

5.1 Overview

This chapter describes the software functional design of CAPS CPU 1. CAPS CPU 1 software is divided into two separate programs: PROM and RAM. The PROM program is CPU 1 software that has been programmed into PROM. This software is fixed and will never change during the course of the Cassini mission. Patches to the PROM software or an entire new program may be developed and uplinked to the spacecraft.

RAM software is stored on the spacecraft solid state recorder (SSR) and transferred to CAPS via ALF blocks. This software will be updated and revised during the Cassini mission as science requirements change.

5.2 Initialization

5.2.1 PROM

Figure 5.2-1 illustrates the power on sequence for CAPS. CAPS begins by testing local and shared RAM. The results of this test are reported in the BIU discrete bits. CAPS then checks the BIU discrete command bits to determine the boot address. It establishes pointers to the correct memory location for the boot and decompresses the PROM into RAM memory. The structure for the compressed image is described in Table 5.2-1. It performs a checksum of the PROM images as it decompresses the program. The checksum is compared with the checksum stored in PROM. The results are reported in the BIU discrete status bits. It finally transfers control to the RAM image.

Table 5.2-1 Compressed PROM Code Structure

Field	Size	Description
Control Word	16 Bits	
Decompression Control Flag	1 Bit (Bit 0)	0 – The following data block is repeated Count times
		1 – There are Count unique blocks following
COUNT	8 Bits (Bits 8-15)	This field is a count. Its meaning is determined by the Decompression Control Flag.
Data Block	Variable (Count * 17)	
Memory Block	17 Words	
Memory Address	16 Bits	The physical address of the following 16 words divided by 16.
Memory Data	16 Words	Sixteen words of data to be copied into RAM.

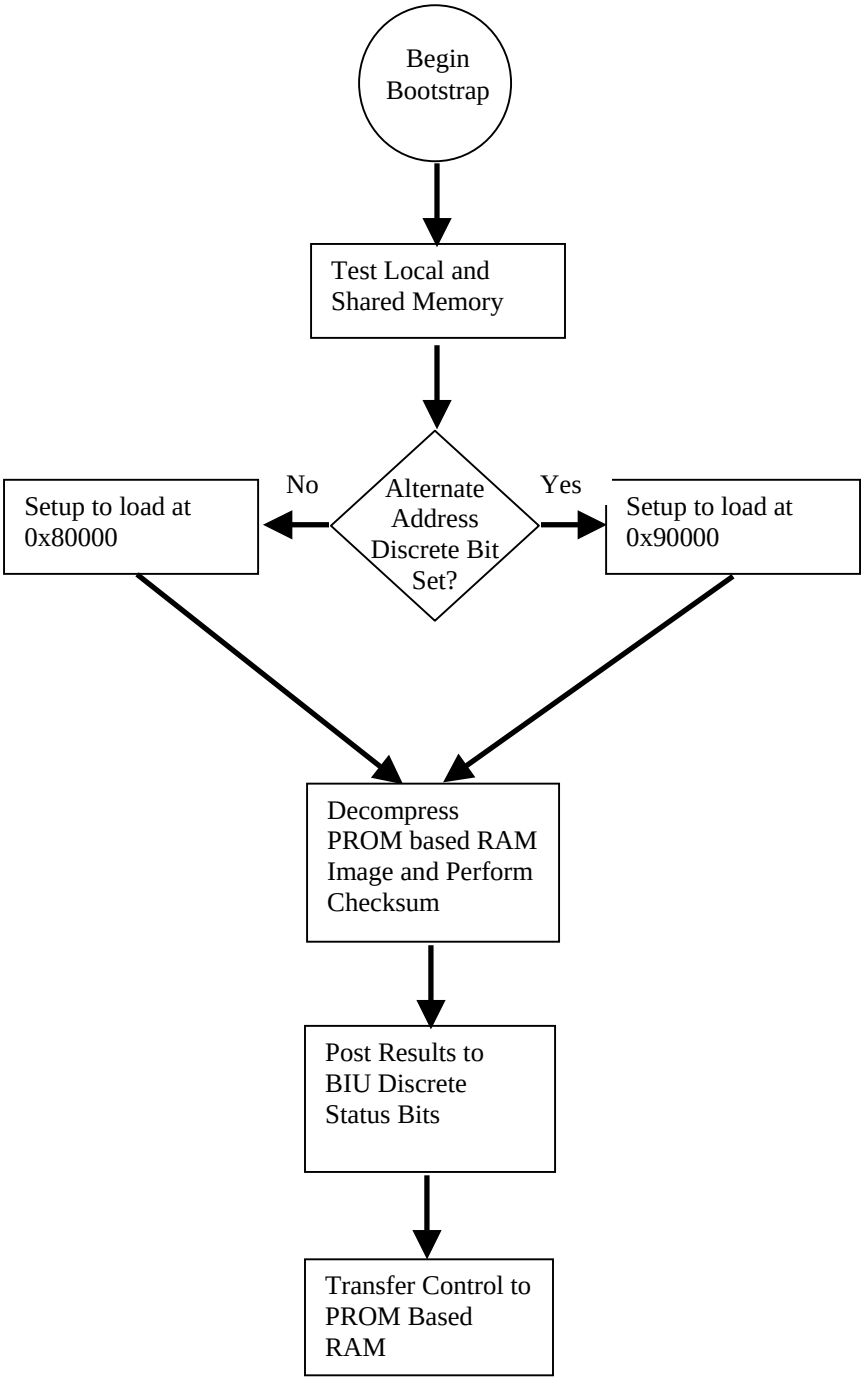


Figure 5.2-1 PROM Boot Strap Flowchart

Figure 5.2-2 illustrates the CAPS modifications to the Tartan Ada runtime initialization. The 1750A processor registers are first initialized for the Tartan Ada environment. The BIU discrete command bits are then checked. If the alternate address bit is set (execute from 0x90000), the memory map registers are fixed up by adding 0x10 to all registers that contain an address page in the range 0x80 to 0x8F. Finally, control is transferred to the Tartan Ada startup code.

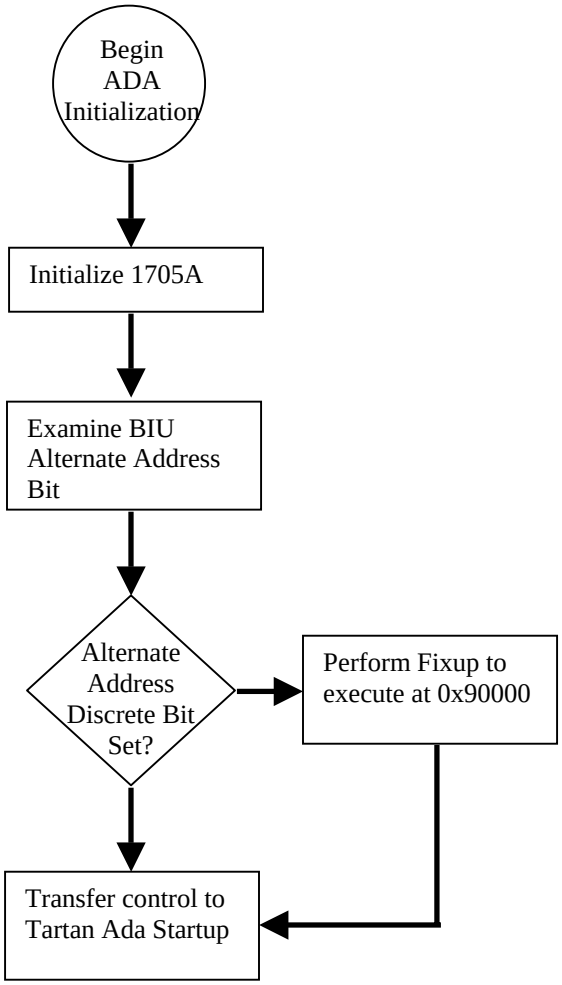
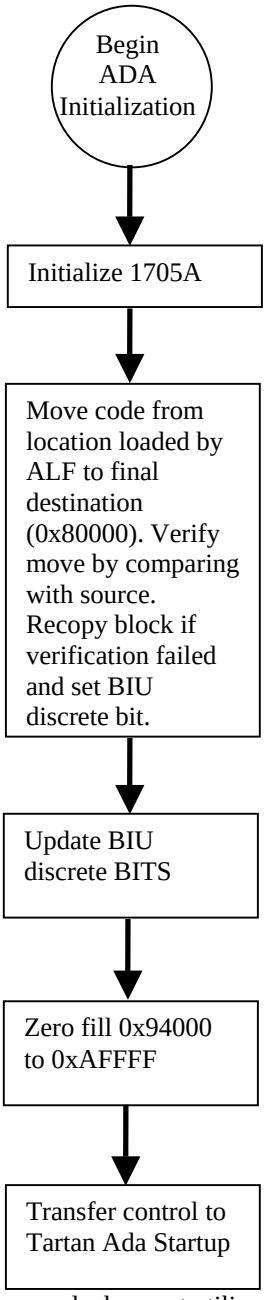


Figure 5.2-2 PROM Ada Initialization Flowchart

5.2.2 SSR Sourced

Figure 5.2-3 illustrates the SSR sourced software initialization. The software begins by initializing the 1750a processor. It then copies and verifies the code loaded into RAM by the previous ALF load Next, it updates the BIU discrete status bits based on the success of the copy and zero fills RAM in the range from 0x94000 to 0xAFFFF. Finally, control is transferred to the Tartan Ada startup code.



Note: The SSR sourced boot strap code does not utilize the alternate address BIU discrete bit.

Figure 5.2-3 RAM Ada Initialization Flowchart

5.3 Interrupt Processing

Interrupts are first handled by an assembly language entry procedure. This entry procedure establishes a stack for the interrupt handler, preserves the 1750A registers and calls the appropriate Ada interrupt handler. After returning from the Ada interrupt routine, it restores the stack pointer, 1750a registers and returns to the code that was interrupted.

5.3.1 RTI

In addition to the interrupt setup performed by the assembly language entry routine, the entry routine also checks if the interrupt has already occurred and prevents the Ada routine from being called again. If an RTI was already active, it increments an EXTRA_RTI count and returns.

The PROM Ada interrupt routine performs the following tasks when an RTI occurs:

- Before the first Collection Repeat Cycle (CRC), perform synchronization to CRC.
- Set Timer A for the DTSTART interrupt.
- Check and process changes to the BIU power bits.
- Check for and process messages in subaddress 29.
- Check for and process messages in subaddress 9.
- Check for and process messages in subaddress 8.
- Check for and process messages in subaddress 7.
- Send Housekeeping and Science Data to subaddresses 12 and 11, respectively.

The RAM Ada interrupt routine performs the following tasks when an RTI occurs:

- Before the first Collection Repeat Cycle (CRC) perform synchronization to CRC.
- Set Timer A for the DTSTART interrupt.
- Check and process changes to the BIU power bits.
- Check for and process messages in subaddress 29.
- Check for and process messages in subaddress 9.
- Check for and process messages in subaddress 8.
- Check for and process messages in subaddress 7.
- Check for and process Ancillary data on subaddress 10.
- Update actuator temperature compensation
- Check if BIU watchdog expired. If the instrument is executing in normal science, then safe the instrument.
- Send Housekeeping and Science Data to subaddresses 12 and 11, respectively.

5.3.2 DTSTART

The DTSTART Ada interrupt handler performs the following tasks for PROM:

- Set Timer A for an RTI Watchdog
- Before synchronization on RTI 7 check for CRC and arm the synchronization circuit if it is a CRC
- After synchronization on RTI 7 switch the BIU transmit buffers
- After synchronization, CPU 2 is released and CPU 2 has commands on RTI 7 send an interrupt to CPU 2 to read its commands.
- Every RTI switch receive buffers.

The DTSTART Ada interrupt handler performs the following tasks for RAM:

- Set Timer A for an RTI Watchdog
- Before synchronization on RTI 7 before the CRC, arm the synchronization circuit
- After synchronization on RTI 7 of every fourth second, arm the synchronization circuit
- After synchronization on RTI 7 switch the BIU transmit buffers
- After synchronization, CPU 2 is released and CPU 2 has commands on RTI 7 send an interrupt to CPU 2 to read its commands.
- Every RTI switch receive buffers.

5.3.3 ACT/Sample Clock

The PROM actuator interrupt handler performs the following tasks:

- Setup for the next A/D conversion
- Update the actuator
- Read the last A/D conversion
- Count actuator interrupts
- Perform A-Cycle boundary processing
  - Increment elapsed A-Cycles
  - Execute A-Cycle boundary commands
  - If a CRC, set the CPU 2 sixty four second flag
  - If a low power transition is pending and it is an odd A-Cycle then transition to low power

The RAM actuator interrupt handler performs the following tasks:

- Acquire data from IBS
- Sweep IBS high voltage supply
- Sweep IMS high voltage supply
- Update the actuator
- Setup for the next A/D conversion
- Acquire Data from ELS
- Count actuator interrupts
- One second before an A-Cycle begins perform:
  - Switch ELS data compression and transmit buffers
  - Switch IBS data compression and transmit buffers
  - Switch actuator data compression and transmit buffers
- Perform A-Cycle boundary processing
  - Switch ELS data acquisition buffers
  - Switch IBS data acquisition buffers
  - Switch actuator data acquisition buffers
  - Increment elapsed A-Cycles
  - Execute A-Cycle boundary commands
  - If A B-Cycle is beginning, execute B-Cycle commands
  - If a CRC, set the CPU 2 sixty four second flag
- Read the last A/D conversion

5.3.3.1 Actuator

For PROM, CAPS must be in either low power or maintenance modes. The BIU power bits are not recognized by the PROM software. The PROM actuator interrupt handler performs the following tasks:

- Every 128 or 256 interrupts (depending on STM), acquire an actuator position sample
- Get the next actuator Phase A and Phase B values
- Compute the current actuator position from the actuator position sample
- Perform actuator processing based on the actuator state and MODE
  - MAINT Mode
    - Sweep the range specified by the two limits twice and then park
  - RAM Mode
    - Position the actuator at limit 1 and hold the position
  - PARK Mode
    - Position the actuator at limit 1 and turn off the actuator
  - RUN State
    - Check the limits and change to the ACCEL/DECEL state when a limit has been reached
    - Increment the number of times a limit is reached if the mode is MAINT
  - START State
    - Begin accelerating and running in the positive direction towards limit 1
  - STOP State
    - Position the actuator on at the beginning of the data table (4 degree boundary)
    - Turn off the actuator
  - ACCEL/DECEL State
    - Perform simple acceleration/deceleration of the actuator
    - At the limit stop and reverse direction

For RAM, CAPS must be in normal science mode with the BIU power bits are set to OPWART. The RAM actuator interrupt handler performs the following tasks:

- Every 128 interrupts, acquire a actuator position sample
- Check the BIU power bits, if the power bits are no long OPWART then park the actuator.
- Get the next actuator Phase A and Phase B values
- Compute the current actuator position from the actuator position sample
- Perform actuator processing based on the actuator state
  - RUN ->
    - check the limits and set the state to decelerate if necessary
  - DECELARATE ->
    - check the limits and change direction and accelerate if the limit has been reached
    - Otherwise adjust for data index for deceleration by using the accel/decel table
  - ACCELERATE ->
    - Adjust the data index for acceleration by using the accel/decel table
    - Change to running state when the accel/decel table is finished
  - PARK MODE ->
    - Check the limits and set the state to decelerating to stop when necessary
  - Decelerating to Stop ->
    - Check the limits; If at or beyond the limit then set the state to stop
  - RAM MODE ->
    - Check the limits and set the state to decelerate to hold when necessary

- DECELERATE TO HOLD ->
  - Check the limits and set the state to hold when necessary
- HOLD ->
  - Continue to write out the last actuator position
- STOP ->
  - Wait until the data index is at the beginning of the actuator data
  - Disable the actuator and turn off power

5.3.3.2 IBS

IBS data acquisition occurs every sample clock period. The details of acquisition and sweeping are discussed in the following paragraphs.

5.3.3.2.1 Acquisition

IBS data acquisition involves:

- Clearing the compression buffer when a telemetry rate change occurs
- Checking to be sure IBS data product generation is enabled
- Checking to be sure the operating mode is Normal Science
- Checking to be sure the power mode is not Sleep
- Acquiring the three words of data from IBS
- Performing dead time correction if it is enabled using the equation:
  SAMPLE / (1.0 – SAMPLE * 1.258045640726E-4)
- Performing threshold detection by testing summed channels:
  - Performing dead time correction
  - Summing over adjacent channels and test the sum against a specified threshold level
  - The threshold is exceeded when the test sum exceed the threshold K_l level for N_s successive samples during M_s successive energy sweeps.
  - If the threshold has been exceeded, then stop sweeping the ESA and bring the ESA voltage to 0.0V
- Perform solar wind beam detection
- Perform solar wind beam tracking

5.3.3.2.2 High Voltage Supply Sweeping

The IBS high voltage stepping uses two step tables: IBS Sweep DAC Table and IBS Sweep Index Table. The IBS Sweep DAC Table contains 852 DAC values in the energy range 1eV to 50eV in 1.67% steps. The IBS Sweep Index Table contains 256 indices into the IBS Sweep DAC Table. The IBS Stim Table is a table of stim frequencies that are written to the IBS. There are several predefined sweep tables:

Solar wind search table
Magnetosphere table 1
Magnetosphere table 2

A 256 standard mode step table is built when the 82IBS_MODE command is received. A solar wind track table is built in real-time to adjust the sweep to track the solar wind beam.

IBS high voltage sweeping involves:

- Checking to be sure the step occurs during the IBS dead time

- Checking to be sure the operating mode is Normal Science
- Checking to be sure the power mode is not Sleep
- Checking the stim flag and performing stim if the stim table is not zero
- Stepping to the next voltage as specified by the Step Index Table.
- Setting the high voltages to zero if the sweep has been disabled or the mode has transitioned from Normal Science
- Acquiring IBS DAC range bits for housekeeping
- Acquiring the peak ESA sweep value for an A-Cycle
- If either the solar wind track table or standard model need to be built, build the next step in the table

5.3.3.3 ELS

ELS data acquisition occurs every fourth sample clock period. It involves:

- Clearing the compression buffer when a telemetry rate change occurs
- Checking to be sure ELS data acquisition is enabled
- Checking to be sure the operating mode is Normal Science
- Checking to be sure the power mode is not Sleep
- If the operate mode is not Normal Science mode or the power mode is Sleep
  - set the ELS mode to A and the lowest voltage setting
- If the instrument is in normal science and was in sleep mode and is not in sleep power mode
  - Restore ELS to its previous state
- Acquiring the eight words of data from ELS
- Performing dead time correction if it is enabled using the equation:
  SAMPLE / (1.0 – SAMPLE * 2.133287823193E-5)
- Performing threshold detection using two methods:
  - Method 1 – Testing Individual Channels:
    - Perform dead time correction
    - Threshold has been exceeded when N_c sucessive samples of each channel are above the threshold K_4 for M_c successive energy sweeps
  - Method 2 – Testing Summed Channels
    - Performing dead time correction
    - Summing over adjacent channels and test the sum against a specified threshold level
    - The threshold is exceeded when the test sum exceed the threshold K_1 level for N_s successive samples during M_s successive energy sweeps.
    - If the threshold has been exceeded, then stop sweeping the ESA and bring the ESA voltage to 0.0V
  - If the threshold was exceeded by either Method 1 or Method 2 then set the ELS mode to A to disable sweeping.

5.3.3.4 HVPS

5.3.3.4.1 HVU-2 ESA Sweeping

HVU-2 ESA sweep occurs every eighth sample clock period. It involves:

- Checking the IMS integrate flag
- Checking to be sure the operating mode is Normal Science, CPU 2 is released, the power mode is not Sleep, and IMS data acquisition is active and sweeping is enabled.
- Checking if sweeping is enabled and background processing is active

    - Set the ESA supply to its lowest level
- Checking if sweeping is enabled and no background processing is going on
    - Write out the next DAC value to the ESA DAC
- Checking if the ESA was sweeping and we have transitioned to low power mode, sleep mode or sleep power mode
    - Set the ESA supply to its lowest level
- Getting the range bits from the DAC for housekeeping
- Getting the peak ESA DAC value for an A-Cycle

5.3.3.4.2 Monitor Acquisition

Acquiring housekeeping monitor data occurs every actuator sample clock interrupt. It involves:

- Setting up the A/D converter
    - Writing out the next MUX value to the MUX located on the HVPS board
    - If the monitor is ELS then writing the next ELS MUX value to ELS
    - Increment the next monitor to sample
    - If the monitor is ELS then run through all ELS monitors before incrementing the next MUX
- Reading the last sample and starting the next conversion
    - Reading the ADC and storing the data in an array of monitors
    - Peforming filtering of monitor data (not ESA data) by averaging the last three samples (~1 second)
    - Processing IBS ESA trickle down monitor in RAM software
    - Processing HVU-2 ESA trickle down monitor in RAM software
    - Incrementing the next monitor to sample
    - If the monitor is ELS then run through all ELS monitors before incrementing

Table 5.3-1 ADC MUX Values

Value	Description	Value	Description
0	Not Used	16	IBS ESA Monitor
1	Not Used	17	IBS CEM Monitor
2	Not Used	18	IBS Temperature Monitor
3	Not Used	19	Actuator Microswitch Position
4	Not Used	20	Actuator 5V Monitor
5	Not Used	21	Actuator 20V Monitor
6	Not Used	22	Actuator Conversion Monitor
7	- 5.2V Supply Monitor	23	Not Used
8	LVPS Current Monitor	24	ELS Monitor
9	+8V Monitor	25	HVU-1 Retarding HV Monitor
10	–8V Monitor	26	HVU-1 Accelerating HV Monitor

11	+5 V Monitor	27	HVU-2 ESA HV Monitor
12	+5V Analog Monitor	28	HVU-2 ST MCP HV Monitor
13	+15V Monitor	29	HVU-2 LEF Monitor
14	-15V Monitor	30	HVU-2 Temperature Monitor
15	LVPS Temperature Monitor	31	Actuator Temperature Monitor

Table 5.3-2 ELS Monitor Channels

Channel	Signal	Source	Scale	Nominal Level
0	+15 V Monitor	Sensor	1 V = 4.6 V	15V = 3.27V
1	Sweep High Voltage Monitor	Sensor	1 V = 1 kV	
2	MCP High Voltage Monitor	Sensor	1 V = 1 kV	
3	MCP Current Monitor	Sensor	1 V = 10 µA	
4	MCP Temperature Monitor	Sensor	TBD	25 C = 1.5V
5	HV Enable/Disable Monitors	Sensor		0 V: All off 1.5V: Sweep on 3.0V: MCP on 5.0V: Both on
6	Not used			
7	Stim. Pulse Ampl. Monitor	SMU	1V = 23 mV	0 (Variable)

5.3.4 CPU 2 IRQ

The CPU 2 IRQ is generated by CPU 2 when a inter-processor command from CPU 2 is in CPU 1's command queue for processing. For PROM, processing CPU 2 IRQ involves:

- Processing the Shared RAM Fail command by setting a global variable to indicate CPU 2 shared RAM failed its test and re-initializing shared memory.
- Processing the Shared RAM Pass command by setting a global variable to indicate CPU 2 shared RAM passed its test and re-initializing shared memory.
- Processing the SAM RAM Fail command by setting a global variable to indicate CPU 2 SAM RAM failed its test.
- Processing the SAM RAM Pass command by setting a global variable to indicate CPU 2 SAM RAM passed its test.
- Processing the Local RAM Fail command by setting a global variable to indicate CPU 2 Local RAM failed its test.
- Processing the Local RAM Pass command by setting a global variable to indicate CPU 2 Local RAM passed its test.
- Processing the ROM Fail command by setting a global variable to indicate CPU 2 ROM failed its test.
- Processing the ROM Pass command by setting a global variable to indicate CPU 2 ROM passed its test.
- All other inter-processor commands are ignored.

For RAM, processing CPU 2 IRQ involves:

- Processing the Shared RAM Fail command by setting a global variable to indicate CPU 2 shared RAM failed its test and re-initializing shared memory.
- Processing the Shared RAM Pass command by setting a global variable to indicate CPU 2 shared RAM passed its test and re-initializing shared memory.

- Processing the SAM RAM Fail command by setting a global variable to indicate CPU 2 SAM RAM failed its test.
- Processing the SAM RAM Pass command by setting a global variable to indicate CPU 2 SAM RAM passed its test.
- Processing the Local RAM Fail command by setting a global variable to indicate CPU 2 Local RAM failed its test.
- Processing the Local RAM Pass command by setting a global variable to indicate CPU 2 Local RAM passed its test.
- Processing the ROM Fail command by setting a global variable to indicate CPU 2 ROM failed its test.
- Processing the ROM Pass command by setting a global variable to indicate CPU 2 ROM passed its test.
- Processing the B-Cycle Starting command by setting a flag used to initiate B-Cycle command processing.
- Processing the Process Background command by checking to be sure background processing is enabled and setting a flag to initiate background processing.
- Processing the Threshold Exceeded command
  - Setting the IMS threshold exceeded error bit in housekeeping
  - Disabling IMS sweeping
  - Setting the HVU-2 ESA to 0 volts.

5.4 Housekeeping Data Processing

Housekeeping telemetry is generated and sent to the BIU during the last second of the collection repeat cycle (at the end of an odd A-cycle). Both BIU transmit buffers are filled with the housekeeping telemetry packet. CDS can then pickup the telemetry from either buffer at any time during the CRC. Two housekeeping data stream formats are generated: (1) maintenance and (2) science. Maintenance housekeeping is produced only by the PROM software during a maintenance STM (IM_40 and IM_40_ALT1) or when commanded by the 82DPU_HK_FORMAT command. For housekeeping parameters that report hardware values, the hardware is read during housekeeping generation when possible to report actual hardware values. The following paragraphs discuss the details of generating housekeeping for the various instrument subsystems. See Appendices I and L for a description of the maintenance and science housekeeping data streams.

5.4.1 Actuator

Generating actuator science housekeeping involves reporting:

- Launch Latch Status (only indicates change immediately after release)
- Actuator execution state
- Actuator temperature compensation state
- Actuator wobble compensation state
- Actuator field of view position 1 and position 2
- Actuator operating mode
- Actuator conversion monitor divided by 16
- Actuator temperature monitor divided by 16
- Actuator 5V monitor divided by 16
- Actuator 20V monitor divided by 16
- Actuator update rate
- Actuator position monitor
- Supplemental heater state

Actuator maintenance housekeeping reports science housekeeping parameters with sampled actuator position data.

These parameters are generated from either CAPS global data or flags contained within the actuator package. Monitor values are retrieved from the data collected by the HVPS monitor acquisition interrupt handler.

5.4.2 CPU 2

CPU 2 housekeeping is divided into two parts: (1) hardware housekeeping and (2) software housekeeping. It is the responsibility of CPU 2 PROM and RAM software to update these housekeeping parameters. CPU 1 retrieves the current housekeeping values from shared memory and adds the structures to the housekeeping telemetry packet. See GSFC document CPU2 Flight Software Functional Design Document for a description of CPU 2 housekeeping generation.

5.4.3 IBS

Generating IBS housekeeping involves reporting:

- ESA peak DAC and range bits
- High voltage power status
- CEM peak DAC
- STIM channel setting
- STIM Control state
- STIM frequency setting
- ESA peak monitor and range bits
- Traffic state (IBS acquisition state)
- High voltage safe/arm state
- High voltage enable/disable state
- CEM high voltage monitor divided by 16
- Temperature monitor divided by 16
- Current sweep table index
- Sweep monitor trickle
- Dead time adjustment state
- Sweep skip value
- Sweep index start

These parameters are generated from either CAPS global data or flags contained within the IBS package. Monitor values are retrieved from the data collected by the HVPS monitor acquisition interrupt.

5.4.4 ELS

Generating ELS housekeeping involves reporting:

- +15V power status
- Dead time period
- Dead time control
- Grid Control
- Sweep Length
- Sweep control
- High voltage control
- Preset adjust
- dE/E control
- High voltage state monitor
- MCP high voltage adjust

- MCP high voltage control
- STIM mode
- STIM control
- STIM adjust
- +15V monitor divided by 16
- MCP high voltage monitor divided by 16
- MCP current monitor divided by 16
- MCP temperature monitor divided by 16
- Traffic state (ELS data acquisition state)
- Mode
- Sweep monitor
- Sweep monitor trickle
- ELS Sum/Average State

These parameters are generated from either CAPS global data or flags contained within the ELS package. Monitor values are retrieved from the data collected by the HVPS monitor acquisition interrupt.

5.4.5 HVPS

Generating HVPS housekeeping involves reporting:

- IMS data acquisition state
- HVU-1 power 1 and power 2 switch states
- HVU-1 enable/disable control state
- HVU-1 safe/arm state
- HVU-1 retarding voltage DAC
- HVU-1 accelerating voltage DAC
- HVU-1 retarding voltage monitor divided by 16
- HVU-1 accelerating voltage monitor divided by 16
- HVU-2 ESA sweep counter
- HVU-2 power state
- HVU-2 enable/disable control state
- HVU-2 safe/arm state
- HVU-2 ST MCP DAC
- HVU-2 LEF MCP DAC
- HVU-2 ESA range and DAC value
- HVU-2 ST MCP monitor divided by 16
- HVU-2 LEF MCP monitor divided by 16
- HVU-2 ESA range and monitor value
- HVU-2 ESA sweep trickle
- HUV-2 ESA sweep table id

These parameters are generated from either CAPS global data or flags contained within the HVPS package. Monitor values are retrieved from the data collected by the HVPS monitor acquisition interrupt.

5.4.6 CPU 1 Software

Generating maintenance housekeeping involves reporting:

- -5.2V monitor divided by 16
- LVPS current divided by 16

- +8v monitor divided by 16
- -8V monitor divided by 16
- +5v monitor divide by 16
- +5v analog monitor divided by 16
- +15V monitor divided by 16
- -15V monitor divided by 16
- LVPS temperature monitor divided by 16
- ELS MCP temperature monitor divided by 16
- IBS temperature monitor divided by 16
- HVU-2 temperature monitor divided by 16
- CPU 1 received command count
- CPU 2 received command count
- CPU 1 rejected command count
- CPU 2 rejected command count
- CPU 1 illegal command count
- CPU 2 illegal command count
- CPU 1 executed command count
- CPU 2 executed command count
- CPU 1 invalid command count
- CPU 2 invalid command count
- CPU 1 last received command
- CPU 2 last received command
- CPU 1 error flags
- CPU 2 error flags
- A Cycle count
- B Cycle count
- Telemetry mode
- CPU 2 state
- CPU 2 health
- CPU 1 shared memory test results
- CPU 2 shared memory test results
- CPU 1 local memory test results
- CPU 2 local memory test results
- CPU 1 ROM memory test results
- CPU 2 ROM memory test results
- CPU 2 SAM memory test results
- CPU 1 watchdog
- Active sequence count
- Last sequence executed
- Data load status flag
- Supplemental heater status
- Instrument Mode change flag
- Spacecraft telemetry mode change flag
- Spacecraft clock status
- Sample clock multiplier
- Instrument power mode
- Instrument operational mode
- Physical telemetry rate
- Logical telemetry rate
- Maintenance housekeeping format
- Housekeeping memory readout

Generating science housekeeping involves reporting:

- -5.2V monitor divided by 16
- LVPS current divided by 16
- +8v monitor divided by 16
- -8V monitor divided by 16
- +5v monitor divide by 16
- +5v analog monitor divided by 16
- +15V monitor divided by 16
- -15V monitor divided by 16
- LVPS temperature monitor divided by 16
- ELS MCP temperature monitor divided by 16
- IBS temperature monitor divided by 16
- HVU-2 temperature monitor divided by 16
- CPU 1 received command count
- CPU 2 received command count
- CPU 1 rejected command count
- CPU 2 rejected command count
- CPU 1 illegal command count
- CPU 2 illegal command count
- CPU 1 executed command count
- CPU 2 executed command count
- CPU 1 invalid command count
- CPU 2 invalid command count
- CPU 1 last received command
- CPU 2 last received command
- CPU 1 error flags
- CPU 2 error flags
- A Cycle count
- B Cycle count
- Telemetry mode
- CPU 2 state
- CPU 2 health
- CPU 1 shared memory test results
- CPU 2 shared memory test results
- CPU 1 local memory test results
- CPU 2 local memory test results
- CPU 1 ROM memory test results
- CPU 2 ROM memory test results
- CPU 2 SAM memory test results
- CPU 1 watchdog
- CPU 2 watchdog
- Active sequence count
- Last sequence executed
- Data load status flag
- Supplemental heater status
- Instrument Mode change flag
- Spacecraft telemetry mode change flag
- Spacecraft clock status
- Sample clock multiplier

- Instrument power mode
- Instrument operational mode
- Physical telemetry rate
- Logical telemetry rate
- Science housekeeping format
- Housekeeping memory readout
- DPU Acquisition configuraiton

5.5 Science Data Acquisition

CPU 1 uses three data acquisition buffers that are “ping-ponged” every A-cycle for ELS and IBS data. CPU 1 acquires the amount of science data as listed in Table 5.5. Data is acquired by the interrupt routine into one buffer. The background compresses acquired data from a second buffer and the RTI interrupt generates science telemetry from a compressed third buffer.

Table 5.5 Data Acquisition Requirements per A-cycle

Source	Cycle	Parameters	# Events/Buffer	# Words/Buffer	Number of Buffers
	A	8 EL x 63 E/Q x 16 AZ	8,064	8,064	3
IBS	A	3 EL x 255 E/Q x 16 AZ	12,240	12,240	3
ACT	A	Position: 1/sec	32	32	3
Total # words				20,336	61,008

5.5.1 ELS Data Acquisition

The acquisition of ELS data occurs every 31.25 milliseconds. The ELS sample bit is low during the ELS dead time. Data is valid 100 microseconds after the start of the dead time period. Data acquisition is handled by the ELS acquisition interrupt handler. See paragraph 5.3.3.3 for a detailed description of ELS data acquisition.

5.5.2 IBS Data Acquisition

IBS data acquisition occurs every 7.8125 milliseconds. See paragraph 5.3.3.2 for a description of IBS data acquisition.

5.5.3 ACT Data Acquisition

Actuator data acquisition occurs every 128 actuator sample clocks (once per second). The most recent monitor sample taken by the HVPS monitor acquisition routine for the actuator position monitor is stored in the actuator acquisition buffer along with the state of the actuator limit switches. The actuator limit switches are encoded in the bits two and three of the actuator position sample as follows:

- Limit 1 => 1
- Limit 2 => 2

5.6 Data Product Generation

CAPS produces the (nominal) number of data products as listed in table 5.6. The number of data products produced by CAPS is dependent upon the logical telemetry rate and the state of the source sensor/actuator. If the

source is disabled, no data is acquired from that source and no data product is produced for the source. The space allocated for the data product in a partially filled CCSDS science telemetry packet is zero filled and ZLP's are substituted for the remaining space allocated in the A-cycle telemetry stream for the missing data product (see section 5.7.3.3, Science Telemetry Packet Format).

Table 5.6-1 Data Product Generation by Logical Telemetry

Logical TLM	Number of Data Products	Data Products Generated
16 kbps	9	ELS, IBS, ACT, IMS ION, IMS TOF-LEF, IMS TOF-ST, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
8 kbps	9	ELS, IBS, ACT, IMS ION, IMS TOF-LEF, IMS TOF-ST, IMS TDC SINGLES IMS TDC LOGICALS, Housekeeping
4 kbps	9	ELS, IBS, ACT, IMS ION, IMS TOF-LEF, IMS TOF-ST, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
2 kbps	9	ELS (normal), IBS (Normal), ACT, IMS ION, IMS TOF-LEF, IMS TOF-ST, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
2 kbps S/W	7	ELS (solar wind), IBS (solar wind), ACT, IMS TOF-ST, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
1 kbps	8	ELS (normal) IBS (Normal), IMS ION, IMS TOF-LEF, IMS TOF-ST, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
1 kbps S/W	6	ELS (normal), IBS (Normal), IMS TOF-ST, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
500 bps	5	ELS, IBS, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping
250 bps	5	ELS, IBS, IMS TDC SINGLES, IMS TDC LOGICALS, Housekeeping

CPU 1 generates the ELS, IBS, ACT and housekeeping data products. CPU 2 generates the IMS TOF-LEF, IMS TOF-ST, IMS ION, IMS TDC SING-EL, and IMS TDC SING-LOG data products. CPU 1 can be commanded to produce a Memory Readout (MRO) data product in place of ELS and IBS data products.

5.6.1 Compression

5.6.1.1 16 KBPS

After CPU 1 acquires the sensor data and decomposes the data according to the algorithms given in the data product format sections below, the resulting data words are compressed from 16 bits to 8 bits and then stored in the data product structure. The data in the ELS and IBS data products is compressed using the compression table found in Appendix C.

5.6.1.2 Collapse, Compression and Run-Length encoding

For data rates below 16 kbps, the data may be collapsed before the 16-to-8 compression is performed. The next two paragraphs discuss the collapse algorithms for ELS and IBS. For IBS, data rates below 16 kbps, an additional run-length encoding is performed to the compressed data. A 20 byte header is included in the IBS data Product. See Table 5.6-2.

Table 5.6-2 IBS Data Product Header

Word	Starting Bit	Size	Description	
0	15	8	Data Product Sync	0xB8
0	7	8	Data Product Id	See Table
1	15	16	Compressed Data Product Size	Number of words of data to follow header
2	15	16	Uncompressed Data Product Size	Number of "samples" in the data product
3	15	2	IBS Mode	0 = Solar Wind 1 = Magnetosphere 2 = Standard 3 = Calibration
3	13	1	IBS Sub Mode	Solar Wind: 0 = Search 1 = Track Normal: 0 = Search 1 = Survey
3	12	4	Product Sub-part Counter	
3	8	1	Strategy	0=Normal 1=Solar Wind
3	7	8	Unused	
4	15	16	Background Level Fan 1	
5	15	16	Background Level Fan 2	
6	15	16	Background Level Fan 3	
7	15	10	Starting Energy	
7	5	6	Subcycle counter	
8	15	6	Peak Energy Index, A-Cycle	
8	9	2	Detector	
8	7	4	Unused	
8	3	4	Peak Energy Index, Sweep	
9	15	8	Peak Energy Index, Energy Step	
9	7	8	Compression Threshold	
10	15	Var.	Compressed Data	

5.6.1.2.1 ELS

Table 5.6-3 summarizes the format of the ELS data products. Data products below 8 kbps are collapsed as indicated below. The collapsed data may summed or averaged. The setting can be changed using the 82ELS_SUM_AVG command. The default is to sum the data.

Table 5.6-3 ELS Data Products

Data Rate	Energy	Elevation	Azimuth	Σ
250 bps	32	8	2	512
500 bps	32	8	4	1024
1 kbps	32	8	4	1024
1 kbps SW	32	8	4	1024

Data Rate	Energy	Elevation	Azimuth	Σ
2 kbps	63	8	4	2016
2 kbps SW	63	8	4	2016
4 kbps	63	8	8	4032
8 kbps	63	8	16	8064
16 kbps	63	8	16	8064

5.6.1.2.2 IBS

IBS products are collapsed, compressed and run-length encoded as indicated in Table 5.6-4. The following algorithm is used to run-length encode the collapsed and compressed IBS data.

- In 8 kbps, 4 kbps, 2 kbps, 1 kbps, 500 bps and 250 bps, given a threshold value and a data volume limit, IBS shall be compressed using a run length encoding (RLE) of values below the threshold
  - 16 bit values above 7264 counts (0.93 MHz) shall be converted to 8 bit DN 191 (=0xBF=1011 1111)
  - 16 bit values between 7264 counts and the threshold value shall be converted to 8 bit numbers using the current 16 to 8 bit conversion
  - Values below threshold shall be run length compressed using 8 bit data numbers 192 (0xC0 = 1100 0000) to 255 (0xFF =1111 1111).
  - Bits 1 to 5 shall contain the number of sequential data numbers below threshold (1-32 sequential values)
  - Bit 0 shall be an even parity for on-ground identification and correction of single bit errors

- The IBS data is truncated if the compressed data exceeds the data volume limit for the current logical data rate.
  - CPU1 counts the number of 8 bit data numbers generated per A-cycle. When this counter exceeds the data volume limit, CPU1 truncates the data for that A-Cycle.

- CPU1 uses an automatic threshold control (ATC) to set the IBS compression threshold.
  - The threshold value shall be based on the last IBS C-cycle in the same sweep pattern as the current cycle
  - CPU1 approximates the compression threshold when change telemetry rates or IBS modes.
  - When changing collapsed products, the new compression threshold shall be ratio of the previous collapse factor and the new collapse factor.
- Products that are multiple A-Cycle collapses are broken into evenly sized parts and one part of the product is transmitted each A-Cycle.

[1]Long scan data will be telemetered as 255 steps of sweep data at 3.39% spacing followed by the second sweep at 3.39% spacing. This gives an effective spacing of 1.67% for 510 steps. It will be the ground system's responsibility to merge the sweeps into a single 510 step sweep.

Table 5.6-4 IBS Data Product Collapse and Compress Map

Logical TLM	DPU Acquire = Solar Wind					DPU Acquire = Normal				
	IBS Mode= Standard	IBS Mode = Solar Wind		IBS Mode = Magnetosphere		IBS Mode= Standard	IBS Mode = Solar Wind		IBS Mode = Magnetosphere	
		Search	Track	Search	Survey		Search	Track	Search	Survey
250 bps	128 Sweep Collapse, RLE, 16->8 Compress 3x255x1	128 Sweep Collapse, RLE, 16->8 Compress 3x255x1	128 Sweep Collapse, RLE, 16->8 Compress 3x127x2	128 Sweep Collapse, RLE, 16->8 Compress 3x255x1	64 Sweep Collapse, RLE, 16->8 Compress 3x255x1	128 Sweep Collapse, RLE, 16->8 Compress 3x255x1	128 Sweep Collapse, RLE, 16->8 Compress 3x255x1	128 Sweep Collapse, RLE, 16->8 Compress 3x127x2	128 Sweep Collapse, RLE, 16->8 Compress 3x255x1	64 Sweep Collapse, RLE, 16->8 Compress 3x255x1
500 bps	16 Sweep Collapse, RLE, 16->8 Compress 3x255x8	16 Sweep Collapse, RLE, 16->8 Compress 3x255x8	Peak Snap Shot, RLE, 16-8 Compress 3x127x32	16 Sweep Collapse, RLE, 16->8 Compress 3x255x8	16 Sweep Collapse, RLE, 16->8 Compress 3x510x4	16 Sweep Collapse, RLE, 16->8 Compress 3x255x8	16 Sweep Collapse, RLE, 16->8 Compress 3x255x8	Peak Snap Shot, RLE, 16-8 Compress 3x127x32	16 Sweep Collapse, RLE, 16->8 Compress 3x255x8	16 Sweep Collapse (long scan), RLE, 16->8 Compress 3x510x4
1000 bps	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x127x256	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x510x64	32 Sweep Collapse, RLE, 16->8 Compress 3x255x4	32 Sweep Collapse, RLE, 16->8 Compress 3x255x4	32 Sweep Collapse, RLE, 16->8 Compress 3x127x8	32 Sweep Collapse, RLE, 16->8 Compress 3x255x4	32 Sweep Collapse (long scan), RLE, 16->8 Compress 3x510x2
2000 bps	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x127x256	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x510x64	8 Sweep Collapse, RLE, 16->8 Compress 3x255x16	8 Sweep Collapse, RLE, 16->8 Compress 3x255x16	8 Sweep Collapse, RLE, 16->8 Compress 3x127x32	8 Sweep Collapse, RLE, 16->8 Compress 3x255x16	8 Sweep Collapse, RLE, 16->8 Compress 3x510x8
4000 bps	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x127x256	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x510x64	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x127x256	RLE, 16->8 Compress 3x255x128	RLE, 16->8 Compress 3x510x64
8000 bps	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress	RLE, 16->8 Compress

Logical TLM	DPU Acquire = Solar Wind					DPU Acquire = Normal				
	IBS Mode= Standard	IBS Mode = Solar Wind		IBS Mode = Magnetosphere		IBS Mode= Standard	IBS Mode = Solar Wind		IBS Mode = Magnetosphere	
		Search	Track	Search	Survey		Search	Track	Search	Survey
	3x255x128	3x255x128	3x127x256	3x255x128	3x510x64	3x255x128	3x255x128	3x127x256	3x255x128	3x510x64
16000 bps	16->8 Compress 3x255x128	16->8 Compress 3x255x128	16->8 Compress 3x127x256	16->8 Compress 3x255x128	16->8 Compress 3x510x64	16->8 Compress 3x255x128	16->8 Compress 3x255x128	16->8 Compress 3x127x256	16->8 Compress 3x255x128	16->8 Compress 3x510x64

Notes:

1) data product dimensions are for a C-Cycle (8 A-Cycles). To determine the data product dimensions for an A-Cycle, divide the azimuthal dimension by 8 (dimensions are EL x E/Q x AZ).

2) Solar wind track will generate two sweeps of 127 steps. One flyback step is included giving a total of 255 steps per 2 seconds.

5.6.2 Data Product Format

Data products are composed of four fields as shown in Table 5.6-5: the Data Product Synchronization (SYNC) field, the Data Product ID (DPID) field, the science data (DATA) field, and the checksum (CHKSUM) field.

Table 5.6-5 General Data Product Format

SYNC	DPID	DATA	CHKSUM
1 byte	1 byte	64-28,228 bytes	2 bytes

5.6.2.1 SYNC Field

The data product synchronization value is B8 hexadecimal. This value is used by the ground system to identify the start of a data product.

5.6.2.2 DPID Field

The DPID field of the data product format contains a data product identifier. This value uniquely identifies the source sensor/actuator, the length of the data, and the logical telemetry rate in effect at the time of data product generation. Table 5.6-36 and 5.6-7 list the data product ids and data product sizes.

Table 5.6-6 Data Product Id Assignments by Logical TLM

Data Product	16	8	4	2	1	0.5	0.25	Spare
Reserved	0	20	40	60	80	A0	C0	E0
ELS	1	21	41	61	81	A1	C1	E1
IBS	2	22	42	62	82	A2	C2	E2
ELS SW				71	91			
IBS SW				72	92			
IMS ION	4	24	44	64	84	A4	C4	E4
IMS TDC LOG	5	25	45	65	85	A5	C5	E5
IMS TDC SING	6	26	46	66	86	A6	C6	E6
IMS TDC SING SW				76	96			
IMS TDC LOG SW				75	95			
IMS TOF-LEF	7	27	47	67	87	A7	C7	E7

Data Product	16	8	4	2	1	0.5	0.25	Spare
IMS TOF-ST	8	28	48	68	88	A8	C8	E8
IMS TOF-ST SW				78	98			
IMS EVENT-1	9							E9
Spare		29	49	69	89	A9	C9	
IMS EVENT-2	A							EA
Spare		2A	4A	6A	8A	AA	CA	
IMS EVENT-ION	B							EB
Spare		2B	4B	6B	8B	AB	CB	
ACTUATOR	C	2C	4C	6C				EC
ACTUATOR SW				7C				
Spare	3	23	43			A3	C3	E3
Spare							CC	
CPU 1 MRO	D	2D	4D	6D	8D	AD	CD	ED
CPU 2/SAM MRO	E	2E	4E	6E	8E	AE	CE	EE
Housekeeping	F	2F	4F	6F	8F	AF	CF	EF
Housekeeping SW				7F	9F			
Reserved	10	30	50	70	90	B0	D0	F0
Spare	11	31	51			B1	D1	F1
Spare	12	32	52			B2	D2	F2
Spare	13	33	53	73	93	B3	D3	F3
Spare	14	34	54	74	94	B4	D4	F4
Spare	15	35	55			B5	D5	F5
Spare	16	36	56			B6	D6	F6
Spare	17	37	57	77	97	B7	D7	F7
Spare	18	38	58			B8	D8	F8
Spare	19	39	59	79	99	B9	D9	F9
Spare	1A	3A	5A	7A	9A	BA	DA	FA
Spare	1B	3B	5B	7B	9B	BB	DB	FB
Spare	1C	3C	5C		9C	BC	DC	FC

Data Product	16	8	4	2	1	0.5	0.25	Spare
Spare	1D	3D	5D	7D	9D	BD	DD	FD
Spare	1E	3E	5E	7E	9E	BE	DE	FE
Spare	1F	3F	5F			BF	DF	FF

†Product ID's are in hexadecimal representation
*Implementation of these logical telemetry modes is deferred until after launch.

Table 5.6-7 Summary Of Data Products

Data Product Length			
DPID (hex)	Source	LTLM (kbps)	Length (bytes)
1	ELS	16	8,064
2	IBS	16	12,240[2]
4	IMS ION	16	28,224
5	IMS TDC LOG	16	2,016
6	IMS TDC SING	16	4,032
7	IMS TOF-LEF	16	4,096
8	IMS TOF-ST	16	4096
9	IMS EVENT-1	16	TBD
A	IMS EVENT-2	16	TBD
B	IMS EVENT-ION	16	TBD
C	ACT	16	64
D	CPU 1 MRO	16	20,304
E	CPU 2 MRO	16	28,228
F	Housekeeping	16	164
21	ELS	8	8,064
22	IBS	8	4,096[1]
24	IMS ION	8	7,056
25	IMS TDC LOG	8	1,512
26	IMS TDC SING	8	2,016

Data Product Length			
DPID (hex)	Source	LTLM (kbps)	Length (bytes)
27	IMS TOF-LEF	8	4,096
28	IMS TOF-ST	8	4,096
2C	ACT	8	64
2D	CPU 1 MRO	8	12,160
2E	CPU 2 MRO	8	TBD
2F	Housekeeping	8	82
41	ELS	4	4,032
42	IBS	4	2,048[1]
44	IMS ION	4	3,024
45	IMS TDC LOG	4	1,008
46	IMS TDC SING	4	1,008
47	IMS TOF-LEF	4	2,048
48	IMS TOF-ST	4	2,048
4C	ACT	4	64
4D	CPU 1 MRO	4	6080
4E	CPU 2 MRO	4	TBD
4F	Housekeeping	4	82
61	ELS	2	2,016
62	IBS	2	1,024[1]
64	IMS ION	2	1,512
65	IMS TDC LOG	2	504
66	IMS TDC SING	2	504
67	IMS TOF-LEF	2	1,024
68	IMS TOF-ST	2	1,024
6C	ACT	2	64
6D	CPU 1 MRO	2	3,040

Data Product Length			
DPID (hex)	Source	LTLM (kbps)	Length (bytes)
6E	CPU 2 MRO	2	3,040
6F	Housekeeping	2	82
71	ELS	2 SW	2,016
72	IBS	2 SW	4,074[1]
75	IMS TDC LOG	2 SW	64
76	IMS TDC SING	2 SW	504
78	IMS TOF-ST	2 SW	1,024
7C	ACT	2 SW	64
7F	Housekeeping	2 SW	82
81	ELS	1	1,024
82	IBS	1	256[1]
84	IMS ION	1	256
85	IMS TDC LOG	1	504
86	IMS TDC SING	1	504
87	IMS TOF-LEF	1	512
88	IMS TOF-ST	1	512
8D	CPU 1 MRO	1	1280
8F	Housekeeping	1	82
91	ELS	1 SW	1,024
92	IBS	1 SW	2,048[1]
95	IMS TDC LOG	1 SW	64
96	IMS TDC SING	1 SW	128
98	IMS TOF-ST	1 SW	512
9F	Housekeeping	1 SW	82
A1	ELS	0.5	1,024
A2	IBS	0.5	234[1]
A5	IMS TDC LOG	0.5	64

Data Product Length			
DPID (hex)	Source	LTLM (kbps)	Length (bytes)
A6	IMS TDC SING	0.5	504
AF	Housekeeping	0.5	82
AD	CPU 1 MRO	0.5	1,280
C1	ELS	0.25	512
C2	IBS	0.25	54[1]
C5	IMS TDC LOG	0.25	16
C6	IMS TDC SING	0.25	256
CD	CPU 1 MRO	0.25	576
CF	Housekeeping	0.25	82

[1]IBS utilizes a second level of compression. The resulting data product size will not be deterministic. The length indicated above represents the maximum telemetry bandwidth allocated to the data product, i.e. IBS data products may be less than but never exceed the allocated bandwidth. The size does not include a 20 byte IBS header. The total IBS data product size is 12260.

5.6.2.3 DATA Field

The data field includes the compressed science data and in some cases may include flags or parameters associated with the decomposition algorithm.

5.6.2.4 CHKSUM Field

The CHKSUM field contains a checksum calculated over the entire data product. The checksum is calculated on unsigned word boundaries using the End-Around-Carry checksum described by JPL in Appendix A of CAS-3-271. The seed for the checksum is 55AA hexadecimal. The unsigned word checksum is calculated by starting with the seed 55AA and adding the values in the data product unsigned word by unsigned word. Bit 16 (carry bit) is shifted to bit 0 and added to the checksum. As an example, the checksum for a 16 kbps logical telemetry rate ELS data product that contains all zeroes for the science data field would be

55AA + B801 + 0000 + 0000 + ... + 0000 + 0000 = 0DAB.

5.6.3 CPU 1 - 16 kbps Logical Telemetry Rate Data Products

5.6.3.1 ELS Data Product

The ELS data product format for 16kbps is shown in Table 5.6-8.

Table 5.6-8 ELS Data Product Format (16 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	01h
DATA	8,064	8 EL x 63 E/Q x 16 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	8,068	

5.6.3.2 IBS Data Product

The data product format for IBS 16kbps is shown in Table 5.6-9.

Table 5.6-9 IBS Data Product Format (16 kbps)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 02
DATA	12,240	3 EL x 255 E/Q x 16 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	12,262	

5.6.3.3 ACT Data Product

The actuator data product format for 16kbps is shown in Table 5.6-10.

Table 5.6-10 ACT Data Product Format (16 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	0Ch
DATA	64	2 Bytes allocated to each 12-bit position sample and 4 bits of status. Total of 32 position samples
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	68	

5.6.3.4 MRO Data Product

The CPU 1 memory read out data product for 16kbps is shown in Table 5.6-11.

Table 5.6-11 MRO Data Product Format (16 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	0Dh
DATA	4	Memory start address
	20,304	10,152 words of CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	20,312	

5.6.3.5 HK Data Product

The housekeeping product for 16kbps is shown in Table 5.6-12.

Table 5.6-12 HK Data Product Format (16 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	0Fh
DATA	164	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	168	

5.6.4 CPU 1 - 8 kbps Logical Telemetry Rate Data Products

5.6.4.1 ELS Data Product

The ELS data product format for 8 kbps is shown in Table 5.6-13.

Table 5.6-13 ELS Data Product Format (8 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	21h
DATA	8,064	8 EL x 63 E/Q x 16 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	8,068	

5.6.4.2 IBS Data Product

The data product format for IBS 8kbps is shown in Table 5.6-14.

Table 5.6-14 IBS Data Product Format (8 kbps)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 22h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 4096 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 4118 bytes

5.6.4.3 Actuator Data Product

The actuator data product format for 8 kbps is shown in Table 5.6-15.

Table 5.6-15 ACT Data Product Format (8 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h

DPID	1	2Ch
DATA	64	2 Bytes allocated to each 12-bit position sample and 4 bits of status. Total of 32 position samples
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	68	

5.6.4.4 MRO Data Product

The CPU 1 memory read out data product for 8 kbps is shown in Table 5.6-16.

Table 5.6-16 MRO Data Product Format (8 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	2Dh
DATA	4	Memory start address
	12,160	6,080 words of CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	12,168	

5.6.4.5 Housekeeping Data Product

The housekeeping data product is shown in Table 5.6-17.

Table 5.6-17 HK Data Product Format (8 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	2Fh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.5 CPU 1 - 4 kbps Logical Telemetry Rate Data Products

5.6.5.1 ELS Data Product

The ELS data product format for 4 kbps is shown in Table 5.6-18.

Table 5.6-18 ELS Data Product Format (4 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h

DPID	1	41h
DATA	4,032	8 EL x 63 E/Q x 8 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	4,036	

5.6.5.2 IBS Data Product

The data product format for IBS 4kbps is shown in Table 5.6-19.

Table 5.6-19 IBS Data Product Format (4 kbps)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 42h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 2048 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 2070 bytes

5.6.5.3 Actuator Data Product

The actuator data product format for 4 kbps is shown in Table 5.6-20.

Table 5.6-20 ACT Data Product Format (4 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	4Ch
DATA	64	2 Bytes allocated to each 12-bit position sample and 4 bits of status. Total of 32 position samples
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	68	

5.6.5.4 MRO Data Product

The CPU 1 memory read out data product for 16kbps is shown in Table 5.6-21.

Table 5.6-21 MRO Data Product Format (4 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	4Dh
DATA	4	Memory start address
	6,080	3,040 words of CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	6,088	

5.6.5.5 Housekeeping Data Product

The housekeeping data product is shown in Table 5.6-22.

Table 5.6-22 HK Data Product Format (4 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	4Fh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.6 CPU 1 - 2 kbps Logical Telemetry Rate Data Products

The same data shall be acquired as in the 16 kb mode. The data acquisition shall be independent of the logical bit rates.

5.6.6.1 ELS Solar Wind Data Product

The ELS data product format for 2kbps is shown in Table 5.6-23.

Table 5.6-23 ELS Data Product Format (2 kbps S/W)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	71h
DATA	2,016	8 EL x 63 E/Q x 4 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	2,020	

5.6.6.2 ELS Normal Data Product

The ELS data product format for 2kbps is shown in Table 5.6-24.

Table 5.6-24 ELS Data Product Format (2 kbps Normal)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	61h
DATA	2,016	8 EL x 63 E/Q x 4 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	2,020	

5.6.6.3 IBS Solar Wind Data Product

The data product format for IBS 2kbps is shown in Table 5.6-25.

Table 5.6-25 IBS Data Product Format (2 kbps S/W)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 72h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 4074 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 4096 bytes

5.6.6.4 IBS Normal Data Product

The data product format for IBS 2kbps Normal is shown in Table 5.6-26.

Table 5.6-26 IBS Data Product Format (2 kbps Normal)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 62h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 1024 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 1046 bytes

5.6.6.5 Actuator Data Product Solar Wind

The actuator data product format for 2 kbps is shown in Table 5.6-27.

Table 5.6-27 ACT Data Product Format (2 kbps S/W)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	7Ch
DATA	64	2 Bytes allocated to each 12-bit position sample and 4 bits of status. Total of 32 position samples
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	68	

5.6.6.6 Actuator Data Product Normal

The actuator data product format for 2kbps is shown in Table 5.6-28.

Table 5.6-28 ACT Data Product Format (2 kbps Normal)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	6Ch

DATA	64	2 Bytes allocated to each 12-bit position sample and 4 bits of status. Total of 32 position samples
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	68	

5.6.6.7 MRO Data Product

The MRO data product format for 2kbps is shown in Table 5.6-29.

Table 5.6-29 MRO Data Product Format (2 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	6Dh
DATA	4	memory dump start address
	3,040	CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	3,048	

5.6.6.8 HK Data Product Solar Wind

The housekeeping data product is shown in Table 5.6-30.

Table 5.6-30 HK Data Product Format (2 kbps - CPU 1 S/W)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	7Fh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.6.9 HK Data Product Normal

The housekeeping data product is shown in Table 5.6-31.

Table 5.6-31 HK Data Product Format (2 kbps - CPU 1 Normal)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	6Fh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.7 CPU 1 - 1 kbps Logical Telemetry Rate Data Products

The same data shall be acquired as in the 16 kb mode. The data acquisition shall be independent of the logical bit rates.

5.6.7.1 ELS Solar Wind Data Product

The ELS data product format for 1kbps is shown in Table 5.6-32.

Table 5.6-32 ELS Data Product Format (1 kbps S/W)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	91h
DATA	1,024	8 EL x 32 E/Q x 4 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	1,028	

5.6.7.2 ELS Normal Data Product

The ELS data product format for 1kbps is shown in Table 5.6-33.

Table 5.6-33 ELS Data Product Format (1 kbps Normal)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	81h
DATA	1,024	8 EL x 32 E/Q x 4 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	1,028	

5.6.7.3 IBS Solar Wind Data Product

The data product format for IBS 1kbps is shown in Table 5.6-34.

Table 5.6-34 IBS Data Product Format (1 kbps S/W)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 92h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 2048 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 2070 bytes

5.6.7.4 IBS Normal Data Product

The data product format for IBS 1kbps Normal is shown in Table 5.6-35.

Table 5.6-35 IBS Data Product Format (1 kbps Normal)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = 82h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 256 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 278 bytes

5.6.7.5 HK Data Product Solar Wind

The housekeeping data product is shown in Table 5.6-36.

Table 5.6-36 HK Data Product Format (1 kbps - CPU 1 S/W)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	9Fh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.7.6 HK Data Product Normal

The housekeeping data product is shown in Table 5.6-37.

Table 5.6-37 HK Data Product Format (1 kbps - CPU 1 Normal)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	8Fh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.7.7 MRO Data Product

The MRO data product format for 1 kbps is shown in Table 5.6-38.

Table 5.6-38 MRO Data Product Format (1 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	8Dh
DATA	4	memory dump start address
	1,280	CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	1,288	

5.6.8 CPU 1 – 0.5 kbps Logical Telemetry Rate Data Products

The same data shall be acquired as in the 16 kb mode. The data acquisition shall be independent of the logical bit rates.

5.6.8.1 ELS Data Products

The ELS data product format for 0.5 kbps is shown in Table 5.6-39.

Table 5.6-39 ELS Data Product Format (0.5 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	A1h
DATA	1,024	Collapse: 8 EL x 32 E/Q x 4 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	1,028	

5.6.8.2 IBS Data Products

The data product format for IBS 0.5kbps is shown in Table 5.6-40.

Table 5.6-40 IBS Data Product Format (0.5 kbps)

Field	Size (bytes)	Data Organization
HEADER	20	See Table 5.6.2, ID = A2h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 234 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 256 bytes

5.6.8.3 HK Data Product

The housekeeping data product is shown in Table 5.6-41.

Table 5.6-41 HK Data Product Format (0.5 kbps - CPU 1)

Field	Size (bytes)	Data Organization

SYNC	1	B8h
DPID	1	Afh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.8.4 MRO Data Product

The MRO data product format for 0.5 kbps is shown in Table 5.6-42.

Table 5.6-42 MRO Data Product Format (0.5 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	Adh
DATA	4	memory dump start address
	1,280	CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	1,288	

5.6.9 CPU 1 – 0.25 kbps Logical Telemetry Rate Data Products

The same data shall be acquired as in the 16 kb mode. The data acquisition shall be independent of the logical bit rates.

5.6.9.1 ELS Data Product

The ELS data product format for 0.25 kbps is shown in Table 5.6-43.

Table 5.6-43 ELS Data Product Format (0.25 kbps)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	C1h
DATA	512	8 EL x 32 E/Q x 2 AZ
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	516	

5.6.9.2 IBS Data Product

The data product format for IBS 0.25kbps is shown in Table 5.6-44.

Table 5.6-44 IBS Data Product Format (0.25 kbps)

Field	Size (bytes)	Data Organization

HEADER	20	See Table 5.6.2, ID = C2h
DATA	Variable	**Reference** Table 5.6-4 IBS Data Product Collapse and Compress Map for a description of the data product format. Maximum size = 54 bytes
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	Variable	Maximum size = 76 bytes

5.6.9.3 HK Data Product

The housekeeping data product is shown in Table 5.6-45.

Table 5.6-45 HK Data Product Format (0.25 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	CFh
DATA	2	Frame ID 0 – First frame of data 1 – Second frame of data
DATA	82	Housekeeping Data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	88	

5.6.9.4 MRO Data Product

The MRO data product format for 0.25 kbps is shown in Table 5.6-46.

Table 5.6-46 MRO Data Product Format (0.25 kbps - CPU 1)

Field	Size (bytes)	Data Organization
SYNC	1	B8h
DPID	1	CDh
DATA	4	memory dump start address
	576	CPU 1 memory data
CHKSUM	2	Word by word unsigned summation of entire data product.
Total	584	

5.7 Telemetry Generation

5.7.1 Science Data Stream

The organization of the CAPS science data stream is show in Figure 5.7-1. This data stream is produced on an A-Cycle boundary.

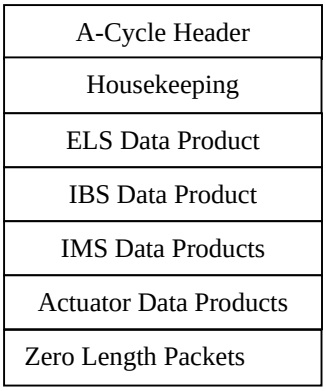


Figure 5.7-1 CAPS Science Data Stream

CAPS begins each data stream with an A-Cycle header. The structure of an A-Cycle header is shown in Table 5.7-1. Following the A-Cycle header is the science data. Housekeeping data is the first in the science data stream. ELS follows the housekeeping data product if it is enabled. ELS is followed by IBS data products, IMS data products and actuator data products. Each of the data products may or may not be present depending on the state of the instrument. Exactly 32,000 words are produced each A-Cycle at the 16 kbps physical telemetry rate, 16,000 words at the 8 kbps physical rate, 8,000 words at the 4 kbps physical rate and 4,000 words in the 2 kbps telemetry rate. Zero length packets are produced until the start of the next A-Cycle.

Table 5.7-1 A-cycle Header Organization

Function	Size (Bytes)	Data Organization
Sync	2	EB90h
A-cycle Counter	1	Counts from 0 to 255 (incremented every A-cycle) and then rolls over.
Data Product Counter	1	Number of data products in this 6-cycle packet.
A-cycle Time Tag	4	CCSDS S/C time format. 32 bit value representing the S/C at beginning of A-cycle (Number of seconds since S/C epoch).
A-cycle Status1	1	Bits 7-6 - TDC singles 13 & 14 selection 5 - CPU2/SAM Mode Change 0 = No 1 = Yes 4 - Background Data 0 = No 1 = Yes 3-0 - Ion Selection Index

Function	Size (Bytes)	Data Organization
A-cycle Status2	1	Bits 7 – Spare 6 – Ion Deadtime Compensation 5-4 – TDC Config. Register #1 (D5 and D4) 3-2 - Molecule/LEF 00 = N/A 10 = LEF Only 01 = Molecule Only 11 = Both 1 – SAM Bkgnd Comp Function 0 = Disable 1 = Enable 0 - Suspect Data Product 0 = No 1 = Yes
A-cycle Status3	1	Bits 7-5 – Spare Bit 4 – ELS Summing And Averaging 0 – Averaging 1 – Summing Bits 3-0 – Data Product Revision
CPU 2's A-cycle Counter	1	A-cycle number within current B-cycle.
Actuator Position	6	Bits 47-36 - A-cycle start + 0 sec 35-24 - A-cycle start + 8 sec 23-12 - A-cycle start + 16 sec 11-0 - A-cycle start + 24 sec
B-cycle Word 1	2	See 5548-FSFD2
B-cycle Word 2	2	See 5548-FSFD2
Checksum	2	Word by word unsigned summation of header.
Total	24	

5.7.2 Housekeeping Data Stream

CAPS produces two different housekeeping data streams: (1) maintenance and (2) science. Each data stream is 88 words in length. The format of the housekeeping data streams are described in Appendix I and K. Science housekeeping is also telemetered in the science telemetry stream as a science data product by the Science Software. Note, the housekeeping data product does not include the CCSDS packet header and is 82 words in length.

5.7.3 CCSDS Packets

The CAPS science data and housekeeping streams are segmented into CCSDS packets before being written to the BIU for pickup by CDS. Depending on the physical telemetry rate either two CCSDS packets containing science telemetry are produced every second or one every four seconds. Once CCSDS packet containing housekeeping is produced either every 64 or 128 seconds depending on the STM. The structure of a CCSDS packet is shown in Figure 5.7-2.

CCSDS PRIMARY HEADER	CASSINI SECONDARY HEADER	PACKET DATA FIELD
48 bits	48 bits	up to 8624 bits

Figure 5.7-2 Cassini CCSDS Packet Format (Overview)

5.7.3.1 CCSDS Primary Header

This section describes the CCSDS Primary Header for CAPS. Figure 5.7-3 shows the fields that define the primary header. The fields are explained below.

Packet Identification					Packet Sequence Control		Packet Length
Version Number	CCSDS Type	Sec. Header Flag	Application Process ID 11 bits		Segment Flags	Source Sequence Count	
			Subsystem ID	Packet Type			
3 bits	1 bit	1 bit	5 bits	6 bits	2 bits	14 bits	16 bits
000	0	1	10100	var	11	var	var

Figure 5.7-3 Cassini CCSDS Packet Primary Header

5.7.3.1.1 Packet Identification

The fields comprising the packet identification of the primary header identifies the format of the telemetry packet and the subsystem/instrument which created the packet.

5.7.3.1.1.1 Version Number

Identifies the version of CCSDS telemetry packets used on Cassini. This three-bit field is always set to a "000".

5.7.3.1.1.2 CCSDS Type

Identifies the packet as a telemetry packet. Always set this one-bit field to a "0".

5.7.3.1.1.3 Secondary Header Flag

Signifies the presence of a secondary header. Always set this one-bit field to a "1".

5.7.3.1.1.4 Application Process Identifier (APID)

Identifies the source of the packet on-board the S/C. The APID is used to differentiate between the various packet types which are created by the S/C subsystems and instruments. This eleven-bit field is split into the following two fields:

Subsystem Identifier – A Five-bit field that identifies the subsystem/instrument which produced the packet. Always set this five-bit field to "10100".

Packet Type – Identifies the type/format/length of the packet. This six-bit value is defined by the subsystem or instrument. The valid Cassini/CAPS packet type identifiers are defined in Table 5.7-2. The CAPS DATA packet types include science data products, memory readout data products and housekeeping data products.

Table 5.7-2 CAPS Packet Types

Packet Type ID	Packet Extension Value (hex)	Size (bits)	Packet Description		
			Data Type	S/C TLM Rate (bps)	Logical TLM Rate (bps)
000001	0D01	8000	CAPS DATA	16000	16000
000010	0D02	8000	CAPS DATA	16000	8000
000011	0D03	8000	CAPS DATA	16000	4000
000100	0D04	8000	CAPS DATA	16000	2000
000101	0D05	8000	CAPS DATA	16000	1000
000110	0D06	8000	CAPS DATA	16000	500
000111	0D07	8000	CAPS DATA	16000	250
010100	0D14	8000	CAPS DATA	2000	2000
010101	0D15	8000	CAPS DATA	2000	1000
010110	0D16	8000	CAPS DATA	2000	500
010111	0D17	8000	CAPS DATA	2000	250
011000	0D18	1408	SCI HK	22	N/A
011001	0D19	1408	MAINT HK	11	N/A
100010	0D22	8000	CAPS DATA	8000	8000
100011	0D23	8000	CAPS DATA	8000	4000
100100	0D24	8000	CAPS DATA	8000	2000
100101	0D25	8000	CAPS DATA	8000	1000
100110	0D26	8000	CAPS DATA	8000	500
100111	0D27	8000	CAPS DATA	8000	250
110011	0D33	8000	CAPS DATA	4000	4000
110100	0D34	8000	CAPS DATA	4000	2000
110101	0D35	8000	CAPS DATA	4000	1000
110110	0D36	8000	CAPS DATA	4000	500
110111	0D37	8000	CAPS DATA	4000	250

5.7.3.1.2 Packet Sequence Control

The Packet Sequence Control fields indicate how the packet is segmented and provide a packet counter.

5.7.3.1.2.1 Segment Flags

The Segment Flags are used to segment long packets. Segmentation is not supported on the Cassini project. Always set this two-bit field to “11”.

5.7.3.1.2.2 Source Sequence Count

A monotonically-increasing count of packets collected with the same APID. The Source Sequence Count is always increased by “1” under nominal conditions. Gaps in the count imply loss of one or more packets. The Source Sequence Count is reset only upon interruption of CAPS, such as a Power-On-Reset (POR) or a processor reset. The Source Sequence Count, a fourteen-bit field, will roll-over after 16,384 packets with the same APID have been produced. (Count is initially “0”.) The count is not increased for zero-length packets (ZLP’s). See section 5.7.4 for a description of ZLP’s.

5.7.3.1.3 Packet Length

Length in bytes (8-bits) of the remainder of the packet following the primary header (i.e., the Secondary Header plus the Data Field). The length is expressed as follows:

Length = {(number of bytes) - 1}.

5.7.3.2 CCSDS Secondary Header

This section describes the CCSDS Secondary Header for CAPS. Figure 5.7.2 shows the fields that define the secondary header. The fields are explained below.

CDS Error Flags				S/C Time
Illegal Length 1 bit	Illegal APID 1 bit	Block Error 1 bit	Error Block ID 5 bits	 40 bits
0	0	0	00000	Var

Figure 5.7-4 Cassini CCSDS Packet Secondary Header

5.7.3.2.1 CDS Error Flags

These flags indicate errors in the transmission of packets through the Information System. The CDS corrects errors in the packet length and part of the APID field if necessary.

5.7.3.2.1.1 Illegal Length

CDS sets this bit to “1” when the length I the packet length field does not correspond to the expected packet length (given the APID). CDS changes the length to the proper value before placing the packet in the transfer frame. Always set this one-bit field to “0”.

5.7.3.2.1.2 Illegal APID

CDS sets this bit to “1” when the packet application process ID does not match the expected application process ID for the packet. CDS only checks and corrects the subsystem ID (first five bits) of the APID. Always set this one-bit field to “0”.

5.7.3.2.1.3 Block Transfer Error

CDS sets this bit to “1” when a status error is detected in one of the 1553B bus messages which transferred the packet or requested the packet. The message which contains the error is identified in the Error Block Identifier. Always set this one-bit field to “0”.

5.7.3.2.1.4 Error Block Identifier

Identifies which 1553B message contains an error flagged by the Block Transfer Error. The blocks used to transfer telemetry packets are all 32 words long, with the exception of the last one, which may be shorter. Because the maximum number of blocks required to transfer a telemetry packet is 17.5, five bits are required to uniquely identify the error-containing message. If multiple errors are detected by CDS, the Error Block ID bits are set to "11111". Always set this five-bit field to "00000".

5.7.3.2.2 S/C Time

The spacecraft time will be the CCSDS Unsegmented Time Code with an arbitrary epoch. The value of the Cassini epoch is 00:00:00 January 1, 1958. This 40-bit field is defined as follows: the first four bytes is the count of the number of seconds past the epoch; the last (fifth) byte provides sub-second timing of approximately four (4) msec resolution. The millisecond resolution field is set to 0. The S/C time field represents the on-board time at which CAPS produced the telemetry packet.

5.7.3.3 Data Field

The packet data field contains CAPS data. The size of this field is dependent on the packet type as defined in Table 5.7-3. Given the packet size from the table, the data field size will be the packet size minus 96 bits (the size of the primary and secondary headers). The formats of the Maintenance Housekeeping Packet and the Science Housekeeping Packet are defined in Appendices I and L. The Science Data Packet is defined in section 5.6

Table 5.7-3 CCSDS Packet Sizes

PACKET SIZES	
Packet Type	**Size in Bytes**
Housekeeping	164
Science	988

5.7.4 Zero Length Packets (ZLP's)

A Zero Length Packet (ZLP) is a packet whose packet length is four or less (see paragraph 5.7.3.1.3). The data field of the CCSDS packet is zero (see paragraph 5.7.3.3). The source sequence count for ZLP does not increment.

5.8 Command Processing

5.8.1 Instrument Commands

The following sections summarizes the CPU1 flight software response to the CAPS commands. See Appendix N for a command summary list and detailed command formats. The command descriptions, discussions, and constraints provided in Appendix N are from the ground system perspective.

CAPS commands are grouped by subsystem, sensor, or function. The command groups are the ACT (actuator), ALF (assisted load format), CPU 1, CPU 2, DPU (data processor unit), ELS, FEE (Front End Electronics), HVU-1, HVU-2, IBS, IMS, MEM (memory), NO_OP (no operation), PS (power system), RT (remote terminal), SAM, SEQ (distributed sequence or IEB), TDC (Time-to-Digital Converter), TRIGGER (sequence trigger), and WRAP. The PS and RT group commands are interpreted by the Cassini power subsystem and the BIU respectively. The WRAP command is interpreted by the ground system. The PS and RT group commands and the

WRAP command are described in Appendix N. The NO_OP command is described under miscellaneous commands in section 5.8.1.13, below.

Instrument commands can be sent to CAPS by the spacecraft via subaddresses 7, 8 or 9 or can be part of a instrument expanded block. The basic format of a command is shown in Figure 5.8-1. CAPS processes commands by first verifying the opcode. Figure 5.8-2 illustrates the command processing logic.

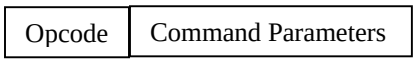


Figure 5.8-1 Instrument Command Format

To ensure safe commanding of high voltage power supplies, commands for the ELS MCP, IBS CEM, IBS ESA, HVU1 Accelerate, HVU1 Retard, HVU2 ESA, HVU2 LEF and HVU2 ST supplies utilize a power supply tolerance table. The structure of the tolerance table is:

Table 5.8-1 High Voltage Tolerance Table Structure

Field	Description
Lower Limit	This is the lower limit of the range to which the tolerance and step size apply. Lower Limit = 0 disables processing.
Tolerance	This is the range of the acceptable voltage specified as a percentage * 100. A tolerance of 0 disables this check.
Step Size	This is the allowable step size between steps of a supply. A step size of 0 disables this check.

The following pseudocode describes the high voltage safety processing:

```
function IS_SAFE (THE_EXPECTED_VALUE, THE_CURRENT_VALUE, CURRENT_DAC, NEXT_DAC, THE_TABLE) is
begin

  if we are step up the voltages then
    for all the entries in THE_TABLE and we haven't found the entry loop
      if THE_TABLE.(I).LOWER_LIMIT > 0 and THE_TABLE(I+1).LOWER_LIMIT > 0
       if THE_EXPECTED_VALUE is 0 or  the expected value is between the current entry and
       the next entry then
         if the tolerance for the current table is 0
           IS_SAFE := TRUE.
           Exit loop
         Else
           If the step size is 0 or NEXT_DAC <= CURRENT_DAC + STEP_SIZE
             Upper Limit = EXPECTED_VALUE + (TOLERANCE/100 * EXPECTED_VALUE)
             Lower Limit = EXPECTED_VALUE - (TOLERANCE/100 * EXPECTED_VALUE)

             If the current value is between Lower Limit and Upper Limit then
                IS_SAFE := TRUE
                Exit loop
             Else
                IS_SAFE := FALSE
                Exit loop
             End if
           End if
         End if
       End if
      End loop
  else
    return IS_SAFE := TRUE
  end if

end IS_SAFE
```

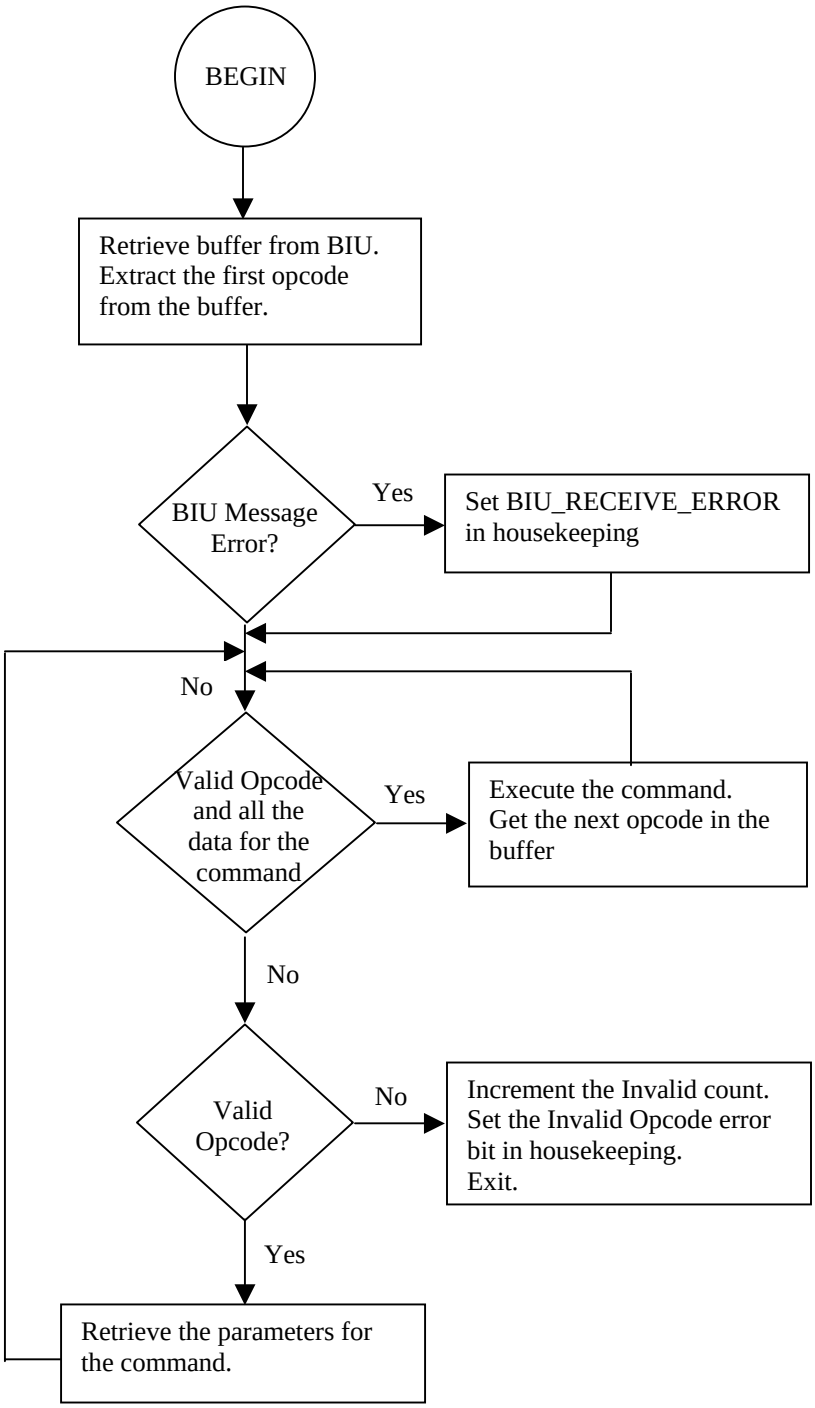


Figure 5.8-2 Command Processing Logic

5.8.1.1 ACT Commands

The ACT commands control the power, activation, and movement of the actuator. There are also commands to control the temperature and "wobble" compensation algorithms associated with the actuator micro-steps. This group contains commands to release the actuator launch latch. See paragraph 4.3.7 for the details of the actuator hardware operation and movement algorithms.

ACT_EXEC **Opcode: 64 (40 hex)**

The actuator execute (ACT_EXEC) command starts or stops actuator operation. CAPS must be in Maintenance, Low Voltage (ROM), or Normal science mode to start the actuator, otherwise this command is marked as illegal and ignored. In Normal Science mode the BIU power interlock bits must be set to OPWART (Operate With ARTiculation) to start the actuator, otherwise this command is marked as illegal and ignored. This command contains a parameter indicating the CAPS time related boundary when the command is executed: immediate or A-cycle. When in Normal Science mode B-cycle is also available.

Note: CPU 2 must be executing its science software in order for a B-Cycle event to be generated.

Upon receipt of an exec command, the field of view mode and limits are used to determine the actuator operation. Upon receipt of a stop command, the actuator is stopped at its current location and power is turned to the actuator is turned off.

The rate parameter determines the speed of the actuator. A rate of 0 corresponds to 1 degree/second. A rate of 1 corresponds to 0.5 degrees/second. A rate of 2 corresponds 0.25 degrees/second and so on. See Appendix N for a complete description of the ACT_FOV parameters.

ACT_FOV **Opcode: 65 (41 hex)**

The actuator field of view (ACT_FOV) command defines the field of view (FOV) limits and the operating mode for the actuator. The processing of this command stores the FOV limits and the mode parameters in software variables used by the ACT interrupt. The field of view limits and operating mode can be changed regardless of the state of the actuator. If the actuator is operating (exec state = start), the transition to the new FOV and mode is immediate. If the actuator is not operating (exec state = stop), the FOV mode and limits are updated and are not applied until an ACT_EXEC command is received.

The minimum FOV is -104 and the maximum FOV is +104 . The FOV is defined in units of 4 , i.e., ±4 , ±8 , ±12 , etc. The FOV limits are constraint checked by the ground system and are not constraint checked by the flight software. To convert the desired field of view to the Limit 1 and Limit 2 parameter range use the equation:

Limit = Desired Limit + 104

This command contains a parameter indicating the CAPS time related boundary when the command is executed: immediate, or A-cycle. When in Normal Science mode B-cycle is also available.

Note: CPU 2 must be executing its science software in order for a B-Cycle event to be generated.

The following actuator modes are currently supported:

- FOV
- PARK
- RAM
- MAINT

The time required to park the actuator is a function of the distance from the current pointing direction to the park position at the time the stop command is executed. See Appendix N for a complete description of the ACT_FOV parameters.

ACT_LAT_CNTRL Opcode: 66 (42 hex)

The actuator latch state (ACT_LAT_STATE), control (ACT_LAT_CNTRL) and activation (ACT_LATCH) commands are used in sequence to release the actuator latch. The ACT_LAT_STATE and ACT_LAT_CNTRL commands help ensure that the actuator latch is not mistakenly released by ground operator command error. A BIU discrete command is required to enable ACT launch latch operations. RT_WTA_ILOCK must be sent for the ACT_LATCH command to take effect. This command is a hardware command. If the thermal wax actuator interlock is not set when this command is issued, no error will be generated.

The ACT_LAT_CNTRL command provides the second level of safety for the activation of the launch latch. The State command parameter indicates whether the launch latch activation control is enabled or disabled. If the control status is disabled, then the ACT_LATCH command is marked as illegal and ignored. If enabled, then the ACT_LATCH command can be accepted. This command is accepted by the flight software in CAPS operating modes MAINT and LOW VOLTAGE (ROM). If CAPS is in any other operating mode then the command is marked as illegal and ignored. This command must be preceded by an ACT_LAT_STATE command that ARM's the latch release function. This command is executed immediately upon receipt.

ACT_LAT_STATE Opcode: 67 (43 hex)

The ACT_LAT_STATE command provides the first of two levels of safety for the activation of the launch latch. The State command parameter indicates whether the launch latch activation is safed or armed. If the launch latch state is SAFEd, then the ACT_LAT_CNTRL and ACT_LATCH commands are marked as illegal and are ignored and the control status is set to DISABLE. If armed, then the ACT_LAT_CNTRL command can be accepted. This command is accepted by the flight software in CAPS operating modes MAINT and LOW VOLTAGE (ROM). If CAPS is in any other operating mode then the command is marked as illegal and ignored. The State command parameter is stored as a software variable and is reported in MAINT housekeeping. This command is executed immediately upon receipt.

ACT_LATCH Opcode: 68 (44 hex)

The ACT_LATCH command releases the actuator launch latch by activating a TWA (Thermal Wax Actuator). The actuator state must be ARM and the control status must be ENABLE for this command to be accepted. This command is accepted by the flight software in CAPS operating modes MAINT and LOW VOLTAGE (ROM). BIU discrete command bit 4 must be set to 1 use 82RT_WTA_ILOCK for this command to take effect. Multiple ACT_LATCH commands are acceptable. If the Power 1 command parameter has the value of ON (1), then the flight software writes a one (1) to location 200C0 (hex). If Power 1 has the value of OFF (0), a value of zero (0) is written to location 200D0 (hex). If the Power 2 command parameter has the value of ON (1), then the flight software writes a one (1) to location 200E0. If Power 2 has the value of OFF (0), a value of zero (0) is written to location 200E0 (hex). This command is executed immediately upon receipt.

ACT_TEMP_COMP Opcode: 69 (45 hex)

The actuator temperature compensation (ACT_TEMP_COMP) command defines whether the temperature compensation algorithm is used during actuator movement. The STATE command parameter is stored as a software variable. If the compensation algorithm state is ENABLE, then the algorithm is used when moving the actuator. If the state is DISABLE, then the algorithm is not used when moving the actuator. The

compensation state defaults to DISABLE upon entering Normal Science Mode. The execution of this command does not depend on the operating state of the actuator. Except after a reset, the last commanded state of the compensation algorithm takes precedence when the actuator articulation is started. This command is executed immediately. The compensation state is reported in SCIENCE housekeeping. This command is not a valid PROM software command. Temperature compensation is not performed during actuator maintenance operation.

ACT_WOBL_COMP Opcode: 70 (46 hex)

The actuator wobble compensation (ACT_WOBL_COMP) command defines whether the wobble compensation algorithm is used during actuator movement. The State command parameter is stored as a software variable. If the compensation algorithm state is ENABLE, then the algorithm is used when moving the actuator. If the state is DISABLE, then the algorithm is not used when moving the actuator. The compensation state defaults to ENABLE upon entering Normal Science mode. The execution of this command does not depend on the operating state of the actuator. Except after a reset, the last commanded state of the compensation algorithm takes precedence when the actuator articulation is started. This command is executed immediately. The compensation state is reported in SCIENCE housekeeping. This command is not a valid PROM software command. Wobble compensation is not performed during actuator maintenance operation.

5.8.1.2 Assisted Load Format (ALF) Commands

Memory loads stored on the SSR are in Assisted Load Format (ALF). This section describes the format, command receipt and processing of an ALF block. Figure 5.8-3 depicts the ALF block format. The Message ID is the Most Significant Word (MSW) and the Odd Word Checksum is the Least Significant Word (LSW).

Message ID
Sequence Number
Segment Number/Total Number
Destination Processor ID
Data Word 0
Data Word 1
Data Word 2
Data ...
Data Word 14
Data Word 15
Even Word Checksum
Odd Word Checksum

Figure 5.8-3 General ALF Block Format

The individual fields of the ALF block are described briefly, below. Reference CAS-3-291, Uplink Formats & Command Tables for a detailed description of the format and use of ALF blocks on the SSR.

Message ID - This field contains command opcode. See the command list in Appendix I for details of the format of the different ALF commands. See below for a summary description of the use of the different ALF blocks.

Sequence Number - This number indicates the order and the location of the ALF block in the SSR memory load partition. This number is used by the CAPS flight software to verify the completeness of the load.

Segment Number - For the ALF (ID = 32) block, the Segment Number is a pointer to the location of the ALF block contents in CAPS memory. The relative address of the first data word in the ALF block can be defined as 16*Segment Number. For the ALF_END (ID = 35) block, the Segment Number equals the total number of ALF blocks contained in the memory load. This includes the number of ALF load blocks, the number of ALF skip blocks, and the ALF terminator block (ALF_END block itself). It does not include the number of blocks skipped in the SSR. For the ALF_SKIP (ID = 37) block, the Segment Number indicates the number of 22-word ALF blocks skipped in the SSR before continuing with good ALF blocks. The ALF_SKIP block is an instruction to the CDS to skip blocks in the SSR. CDS forwards this block to CAPS with the rest of the memory load. CPU 1 adds the skip count (Segment Number) to the current ALF sequence number.

Destination Processor ID - This value identifies the destination processor memory of the ALF block. Shared memory loads have a destination of CPU 1 (ID = 0) and SAM memory loads have a destination of CPU 2 (ID = 1).

Data Word 0 to Data Word 15 -This is a block of 16 words of memory load data.

Even Word Checksum - This value is an end-around carry checksum computed over words 1, 3, 5, 7, ..., etc. of the entire ALF block (ALF block starts with word 1). Starting seed for the checksum is 55AA hexadecimal.

Odd Word Checksum - This value is an end-around carry checksum computed over words 2, 4, 6, 7, ..., etc. of the entire ALF block (ALF block starts with word 1). Starting seed for the checksum is 55AA hexadecimal.

ALF **Opcode: 32 (20 hex)**

The ALF command directs the updating of memory at the location given by the Segment Number parameter with the 16 data words contained in the ALF block. The processor ID parameter indicates whether the ALF command is interpreted by CPU 1 or CPU 2. When CPU 1 receives an ALF block with a processor ID parameter set to CPU 2, the odd and even checksums are calculated and compared with the checksums contained in the ALF block. The ALF block and then stored in the command exchange area of shared memory. If the destination processor is CPU 1, then the odd and even checksums are calculated and compared respectively with the checksums contained in the command. If the checksums match, the 16 words are written to memory at the starting location given by the Segment Number parameter*16. If the checksums do not match, an error bit is set and reported in housekeeping. The ALF block will be processed regardless. The DATA_LOAD housekeeping parameter will be set to ERROR.

The Sequence Number parameter is limit checked by the default range 27,771 to 42,516. This limit range can be changed by the ALF_XTREMES command. The Sequence Number parameter is checked to ensure that it increments with each ALF block received (taking into account any ALF_SKIP blocks) until an ALF_END is received. If a Sequence Number is missed or is out of order, the ALF block is ignored, the Invalid ALF Sequence Number housekeeping error bit is set and the DATA_LOAD flag is set to ERROR. Note that ALF blocks directed to update shared memory have a destination ID of CPU 1 and that SAM memory ALF blocks have a destination of CPU 2. For ALF blocks destined for CPU 2, CPU 2 must be released from reset, otherwise the Invalid System State housekeeping error bit is set and the DATA_LOAD flag is set to error. ALF block commands are accepted in all operating modes. This command is executed immediately.

ALF_END **Opcode: 35 (23 hex)**

The ALF_END command indicates the end of an ALF block load. CPU 1 calculates and checks odd and even checksums. If an error occurs the Invalid ALF checksum housekeeping error bit is set and the

DATA_LOAD flag is set to ERROR. ALF_END commands are accepted in all operating modes. This command is executed immediately.

ALF_RANGE Opcode: 36 (24 hex)

When an ALF load is initiated, the entire CAPS memory load partition is sent to the instrument. The ALF_RANGE command provides a means for the DPU to ignore all but a designated sub-block of the load. This command is used by either CPU 1 or CPU 2 to calculate the range of active ALF blocks to be pulled from the next ALF load. This command is only in effect during the subsequent ALF load. After the range has been used for a load, the range is reset to the default limits or the limits established by an ALF_XTREMES command. This command contains offset and count parameters that enables word boundary resolution of the selected memory block. The relative address of the first data word in the ALF block load is defined as ((16*Segment Number of First Selected ALF Block) + Offset). The relative address of the last data word in the ALF block load is defined as ((16*Segment Number of Last Selected ALF Block) + Count). This command is accepted in all operating modes. This command is executed immediately.

ALF_SKIP Opcode: 37 (25 hex)

The ALF_SKIP command is included in an ALF memory load so that the memory load stored in SSR memory can “skip” over bad SSR memory locations. The ALF_SKIP is forwarded to the instrument during a load by CDS. CAPS flight software discards the skip block but uses the segment number parameter to verify the next ALF data block is in sequence. If the segment number of the ALF_SKIP block is not the next number in sequence, the Invalid ALF Sequence Number housekeeping error bit is set, the ALF_SKIP is ignored and the DATA_LOAD flag is set to ERROR.

ALF_XTREMES Opcode: 38 (26 hex)

This command changes the range of ALF sequence numbers expected during an ALF load. This allows CAPS to gracefully handle the relocation of the CAPS memory load partition on the SSR. The new limits are stored in memory and remain active until another ALF_XTREMES command is received or until a processor reset is executed or another loaded image is executed (i.e. PROM to Science). This command is accepted in all operating modes. This command is executed immediately.

5.8.1.3 CPU 1 Commands

CPU 1 commands are targeted to CPU 1 and are not forwarded to CPU 2.

CPU1_MRO Opcode: 49 (31 hex)

This command initiates the Memory Read Out (MRO) function for CPU 1. Memory read out is in effect for one (1) A-cycle. Normal data acquisition continues but the ELS and IBS data products are replaced by the MRO data product. This command is accepted in all operating modes. This command is an implicit A-cycle command and is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command. It is only valid in normal science mode. The command is marked as illegal when received by the PROM software or other operating modes.

CPU1_RAM_ADDR Opcode: 50 (32 hex)

This command supplies CPU 1 with the beginning address of its RAM resident program. A default address of 90000 (hex) is programmed in PROM and Science software. This command allows a way to change the default address. CPU 1 stores the address to be used with subsequent CPU1_RAM_EXEC command. This

command is valid in Low Power, Low Power (ROM) and CPU2/SAM Ready modes. This command is executed immediately upon receipt.

CPU1_RAM_EXEC Opcode: 51 (33 hex)

This command instructs CPU 1 to begin execution at a default (hardcoded in PROM) RAM address unless the default address has been superceded by the RAM address specified by a previously received CPU1_RAM_ADDR command. Once the RAM program starts execution, the CPU1_EXEC_STA(te) flag is set to “RAM”. This command is valid in Low Power, Low Power (ROM) and CPU2/SAM Ready modes. This command is executed immediately upon receipt.

CPU1_WATCHDOG Opcode: 52 (34 hex)

This command enables the CPU 1 watchdog function. This function is enabled by periodically setting the Terminal Count (TC) counter of the PIC. If the counter expires, the DPU is reset. The state of the CPU 1 watchdog function defaults to DISABLE upon reset. This command is valid in Low Power, Normal Science and Sleep. This command is executed immediately upon receipt.

5.8.1.4 CPU 2 Commands

The CPU 2 commands are CAPS commands that directly effect CPU 2 processing. Some of these commands are interpreted by CPU 1 to hold or release CPU 2 in reset. The rest of the commands are passed to CPU 2 for execution by that subsystem. Only those CPU 2 commands executed by CPU 1 are described in this document. Refer to 5548-FSFD-02 for a description of the remaining CPU 2 commands.

CPU2_CNTRL Opcode: 176 (B0 hex)

This command is interpreted by CPU 1. It is used to hold or release the CPU 2 reset line. When CPU 2 is held in reset, SAM and the TDC are also held in reset. When this command is used to release CPU 2 from reset, CPU 2 will begin executing its PROM based bootstrap program. The housekeeping flag CPU2_EXE_STA is set to ROM. This command is valid in all modes. This command is executed immediately upon receipt.

CPU2_RESET Opcode: 183 (B7 hex)

This command is interpreted by CPU 1. CPU 1 performs a soft reset of CPU 2 by writing a zero (0) to address 10000 hex to reset CPU 2 and then writing a one (1) to address 10000 hex to release CPU 2. Resetting CPU 2 also resets SAM and TDC. CPU 2 starts executing its PROM based code. Housekeeping flag CPU2_EXEC_STA(te) is set to “ROM”. This command is valid in all modes. This command is executed immediately upon receipt.

5.8.1.5 DPU Commands

Unless otherwise indicated, DPU commands effect both CPU 1 and CPU 2. When CPU 1 receives a DPU command that effects CPU 2, the command is passed to CPU 2 for interpretation.

DPU_A_CYCLE Opcode: 160 (A0 hex)

The DPU_A_CYCLE command provides a method of command synchronization within the DPU. Commands that are implicitly A-cycle commands or that have a “Boundary” parameter set to “A_CYCLE” are queued within CPU 1, CPU 2, or both. These commands remain queued for execution until the processors receive this command. This command signals the processors to execute all A-cycle commands that have been queued since the last DPU_A_CYCLE command in the order that the queued commands

were received. The queued commands are executed at the next A-cycle boundary after receipt of this command. Sending this command when no A-cycle commands have been queued has no effect on the DPU and is not considered an error. This command is valid in all modes. This command is executed immediately (placed in the A-Cycle command queue).

DPU_B_CYCLE **Opcode: 161 (A1 hex)**

The DPU_B_CYCLE command provides a method of command synchronization within the DPU. Note that B-cycle commands are primarily targeted to CPU 2. Commands that are implicitly B-cycle commands or that have a "Boundary" parameter set to "B_CYCLE" are queued within CPU 1, CPU 2, or both. These commands remain queued for execution until the processors receive this command. This command signals the processors to execute all B-cycle commands that have been queued since the last DPU_B_CYCLE command in the order that the queued commands were received. The queued commands are executed at the next B-cycle boundary after receipt of this command. Sending this command when no B-cycle commands have been queued has no effect on the DPU and is not considered an error. This command is only valid in Low Power, Normal Science, and Sleep modes. This command is executed immediately (added to the B-Cycle command list).

DPU_ACQ **Opcode: 171 (AB hex)**

This command sets the acquisition and compression strategies for the ELS, IBS and IMS data products. This command only affects the 2 and 1 kbps data products. This command permits a tradeoff of telemetry bandwidth between ELS, IBS and IMS to maximize the scientific value of the data acquired. This command can be executed on either an A-Cycle or B-Cycle boundary and requires an 82DPU_A_CYCLE or 82DPU_B_CYCLE command to force it to execute. The default strategy is NORMAL. . This command is valid in all modes.

DPU_BACKGND **Opcode: 162 (A2 hex)**

This command enables/disables background measurements for both CPU 1 and CPU 2. Background noise is measured by setting all sweeping supplies to their lowest energy level in the fourth (4th) A-cycle during normal data acquisition and data product generation. This measurement is repeated during subsequent B-cycles at an interval defined by the DPU_BKGND_INT command. CPU 2 signals CPU 1 one (1) IMS sample clock before the background B-cycle begins. This command is reflected in housekeeping in the DPU_BKG_CTRL parameter. The A-cycle containing the background data is marked in the A-cycle header in A-cycle Status 1. This command is valid only in Normal Science mode. This command is executed on the next B-cycle boundary following it receipt by CPU 1 and CPU 2. A DPU_B_CYCLE command is not required for this command to be executed.

DPU_BKGND_INT **Opcode: 163 (A3 hex)**

This command defines the background measurement interval for both CPU 1 and CPU 2. Background noise is measured by setting all sweeping supplies to their lowest energy level in the fourth (4th) A-cycle during normal data acquisition and data product generation. This measurement is repeated during subsequent B-cycles at an interval defined by this command. CPU 2 signals CPU 1 one (1) IMS sample clock before the background B-cycle begins. The interval is reflected in housekeeping in the DPU_BKG_INT parameter. The A-cycle containing the background data is marked in the A-cycle header in A-cycle Status 1. This command is valid only in Normal Science mode. This command is executed on the next B-cycle boundary following it receipt by CPU 1 and CPU 2. A DPU_B_CYCLE command is not required for this command to be executed.

DPU_CLEAR_ERRS **Opcode: 164 (A4 hex)**

This command is interpreted by both CPU 1 and CPU 2. This command instructs the processors to clear (set to zero) internal detailed error indicators as well as those reported in housekeeping. Command error counters are also set to zero. This command is valid in all modes. This command is executed immediately upon receipt.

DPU_HK_FORMAT Opcode: 165 (A5 hex)

This command selects the format of the housekeeping stream produced by CPU 1. This command satisfies the JPL requirement of providing Maintenance housekeeping in a “Science” mode (a higher telemetry rate than the maintenance STM). The format of the housekeeping packet is marked in the housekeeping stream in parameter BIU_HKFORMAT. This is needed since the packet type indicates “normal” science housekeeping is contained in the packet. This command is only available in Maintenance, Low Voltage (ROM) modes or CPU2/SAM Ready. If this command is received in any other mode, it is marked as an illegal command and ignored. This command is not passed on to CPU 2. This command is interpreted immediately but the format change do not occur until the next 64-second housekeeping boundary (the next repeat cycle).

DPU_HK_MRO Opcode: 166 (A6 hex)

This command defines the address ranges/table number of the memory locations to be included in the HK MRO. There are 16 words in the HK telemetry packet reserved for a trickled MRO. The intent of this readout is to confirm memory/table contents over time without taking up science data allocation by using the MRO data product. This mechanism also allows visibility into the DPU after a memory/distributed sequence upload. This command is directed to either CPU 1 or CPU 2. Note that SAM memory is mapped into CPU 2's memory space. This command is valid in all modes. If this command is received with a destination of CPU 2 when the CAPS mode has CPU 2 in reset, this command is marked as illegal and is ignored. This command is executed immediately. The effects of the command are seen at the next S/C collection repeat boundary (i.e., a 64-second boundary) when the next housekeeping packet is picked up by CDS. A DPU_A_Cycle command is not required for this command to be executed.

DPU_MODE Opcode: 167 (A7 hex)

This command is interpreted only by CPU 1. This command instructs CPU 1 to put the DPU in a predefined operating mode. When a mode change occurs, housekeeping parameter DPU_MODE_CHG is set to YES for until it is sent once in HK telemetry and then it is set back to NO. The current DPU mode is reflected in housekeeping parameter DPU_MODE. This command is marked as illegal and ignored if the commanded mode is in conflict with the BIU discrete bits (see RT_OPMODE) defining the power envelope in which CAPS must operate. See Figure 3.X-2, State Transition Matrix, for the valid mode transitions. If this command instructs CPU 1 to enter an illegal mode, this command is marked as illegal and is ignored.

DPU_SUPHTR_PWR Opcode: 170 (AA hex)

This command is interpreted only by CPU 1. This command instructs CPU 1 to turn the CAPS supplemental heater on/off. The supplemental heater is turned on during CPU 1 software initialization (defaults to ON). CPU 1 turns the supplemental heater on by writing any value to 20000 hex. CPU 1 turns the supplemental heater off by writing any value to 20010 hex. This command is valid in all modes. This command is executed immediately upon receipt.

DPU_TLM_RATE Opcode: 172 (AC hex)

This command is interpreted by CPU 1. This command changes the CAPS internal logical telemetry rate. This logical rate is used to manage the SSR telemetry data allocation. The logical telemetry rate will always be less than or equal to the S/C telemetry mode (STM). If this command instructs the DPU to enter a

logical telemetry mode that is illegal for the current S/C telemetry mode, the command is marked as illegal and is ignored. The logical telemetry rate effects data product generation. Only the 16 kbps and 2 kbps logical telemetry rates are available for ICO. The logical telemetry rate is reflected in housekeeping by parameter LTLM_RATE. The logical telemetry rate is also evident by the packet ID of the science data stream. If the command's Boundary parameter is A_CYCLE, the telemetry rate is changed on the next A-cycle boundary that is also a S/C collection rate boundary (i.e., a 64-second boundary). If the Boundary parameter is B_CYCLE, the telemetry rate is changed on the next B-cycle boundary. Both boundary choice requires the corresponding DPU_A_CYCLE or DPU_B_CYCLE command.

DPU_TRAFFIC Opcode: 173 (AD hex)

This command is interpreted by both CPU 1 and CPU 2. This command enables/disables one, two, or all three CAPS sensors. All sensors are enabled after a reset by default. Data acquisition is suspended when a sensor is disabled. The sensor status is reflected in housekeeping by parameters ELS_SENSOR, IBS_SENSOR, and IMS_SENSOR. This command is valid only in Normal Science mode. If the command's Boundary parameter is A_CYCLE, the sensor is disabled/enabled on the next A-cycle boundary that is also a S/C collection rate boundary (i.e., a 64-second boundary) following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the sensor is disabled/enabled on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choice requires the corresponding DPU_A_CYCLE or DPU_B_CYCLE command.

5.8.1.6 ELS Commands

The ELS commands are interpreted by CPU 1 to control the power, application of the dead time correction algorithm, stim, and mode of the ELS sensor. See the 5548-ELS and section 0 of this document for the details of the ELS hardware operation.

ELS_DTM_CNTRL Opcode: 80 (50 hex)

The ELS_DTM_CNTRL enables/disables the dead time correction of ELS sensor data. The dead time correction status is held in a local RAM variable and is reflected in housekeeping by parameter ELS_DTM_CTRL. This command is valid only in Normal Science mode. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_DTM_PERIOD Opcode: 91 (5B hex)

The ELS_DTM_PERIOD selects whether the ELS dead time correction function is to be 1/8 or 2/8 of the sample period by sending command word 1 bit 4 set to 0 for 1/8 and 1 for 2/8. The dead time period status is read from the ELS sensor hardware and reported in housekeeping by the parameter ELS_DTM_PERIOD. This command is valid only in Normal Science mode. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_GRID_CNTRL Opcode: 92 (5C hex)

The ELS_GRID_CNTRL specifies whether the ELS Grid is enabled or disabled by sending command word 5 bit 4 set to 0 to disable and 1 to enable. The grid control status is read from the ELS sensor hardware and reported in housekeeping by the parameter ELS_GRID_CNTRL. This command is valid only in Normal Science mode. This command is an implicit A-cycle command. This command will be executed on the A-cycle boundary following the receipt of an DPU_A_CYCLE command.

ELS_HV_PWR Opcode: 93 (5D hex)

This command turns the ELS HV power supply on or off. When commanded to turn the ELS power off, the CPU sends command word 6 bit 1 set to 0. When commanded to turn the ELS power on, the CPU sends command word 6 bit 1 set to 1. It always disables sweeping (command word 3 bit 3), sets the sweep length to 1 step (command word 3 bit 2), sets the sweep preset control to 31 (command word 4 bits 4-0), and sets the sweep dE/E control to 3 (command word 3 bits 1-0). This puts the ELS supply in the lowest safe state. The parameters changed by this command are reflected in the following housekeeping parameters: ELS_HV_PWR, ELS_SWP_LEN, ELS_SWP_CTRL, ELS_HV_CTRL, ELS_PSET_ADJ, and ELS_dE_CTRL. This command is valid only in Normal Science. If this command is received in any other mode it is marked as illegal and is ignored. This command is executed immediately upon receipt.

ELS_MCP_ADJ **Opcode: 82 (52 hex)**

This command supplies the DAC value for the ELS MCP by sending command words 2 bits 4-0 and 6 bit 2 to address 30040 hex. The DAC value is reflected in housekeeping in parameter ELS_MCP_ADJ. This command is valid in Normal Science mode. If this command is received in any other mode it is marked as an illegal command and is ignored. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

ELS_MCP_PWR **Opcode: 83 (53 hex)**

The ELS_MCP_PWR command turns the ELS MCP HV power on or off. When commanded to turn the ELS MCP power off, the CPU sets bit 0 to 0 of command word 6. When commanded to turn the ELS MCP power on, the CPU sets bit 0 to 1 of command word 6 and sets the MCP adjust value to 0 in command word 2. The ELS MCP power status is reflected in housekeeping parameter ELS_MCP_CTRL. This command is valid in Normal Science and Sleep modes. If this command is received in any other mode it is marked as illegal and is ignored. This command is executed immediately upon receipt.

ELS_MODE_A **Opcode: 85 (55 hex)**

The ELS_MODE_A command configures the ELS into mode A via commands to the SMU. This command sets the ELS sweep to disabled, sets the length to 1 step, and sets the dE/E control and preset control values to the corresponding command parameter values. This mode is reflected by the following collective housekeeping parameters: ELS_SHV_CTRL, ELS_SWP_LEN, ELS_dE_CTRL, and ELS_PSET_ADJ. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_MODE_B **Opcode: 86 (56 hex)**

The ELS_MODE_B command configures the ELS into mode B via commands to the SMU. This command sets the ELS sweep to enabled, sets the length to 64 steps. There is no dE/E control or preset control values. This mode is reflected by the following collective housekeeping parameters: ELS_SHV_CTRL, ELS_SWP_LEN, ELS_dE_CTRL, and ELS_PSET_ADJ. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_MODE_C0 **Opcode: 87 (57 hex)**

The ELS_MODE_C0 command configures the ELS into mode C0 via commands to the SMU. This command sets the ELS sweep to enabled, sets the length to 32 steps, sets the dE/E control to 16% and sets the preset control values to the corresponding command parameter value. This mode is reflected by the following collective housekeeping parameters: ELS_SHV_CTRL, ELS_SWP_LEN, ELS_dE_CTRL, and

ELS_PSET_ADJ. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_MODE_C1 Opcode: 88 (58 hex)

The ELS_MODE_C1 command configures the ELS into mode C1 via commands to the SMU. This command sets the ELS sweep to enabled, sets the length to 32 steps, and sets the dE/E control to 16%. There is no preset control value in this mode. This mode is reflected by the following collective housekeeping parameters: ELS_SHV_CTRL, ELS_SWP_LEN, ELS_dE_CTRL, and ELS_PSET_ADJ. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_MODE_D Opcode: 89 (59 hex)

The ELS_MODE_D command configures the ELS into mode D via commands to the SMU. This command sets the ELS sweep to enabled, sets the length to 32 steps, and sets the dE/E control to 25%. There is no preset control value in this mode. This mode is reflected by the following collective housekeeping parameters: ELS_SHV_CTRL, ELS_SWP_LEN, ELS_dE_CTRL, and ELS_PSET_ADJ. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_MODE_E Opcode: 90 (5A hex)

The ELS_MODE_E command configures the ELS into mode E via commands to the SMU. This command sets the ELS sweep to enabled, sets the length to 32 steps, and sets the dE/E control to 36%. There is no preset control value in this mode. This mode is reflected by the following collective housekeeping parameters: ELS_SHV_CTRL, ELS_SWP_LEN, ELS_dE_CTRL, and ELS_PSET_ADJ. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_STIM Opcode: 84 (54 hex)

The ELS_STIM command supplies the amplitude, mode, and state of the ELS stimulator. The amplitude command input is written to the ELS in ELS command word 7 bits 4-2. The mode input is written commanded via word 7 bit 1. The stimulator state is commanded in ELS command word 7 bit 0. These ELS command inputs are reflected in housekeeping parameters ELS_STM_MODE, ELS_STM_CTRL, and ELS_STM_ADJ. This command is valid in Normal Science mode only. If this command is received in any other mode it is marked as illegal and ignored. This command is an implicit A-cycle command. This command will be executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

ELS_SUM_AVG Opcode: 94 (5E hex)

This command is used to set whether the ELS data products are summed or, summed and averaged. By default all ELS data products are summed. This command is an implicit A-cycle command. This command will be executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command. This command is valid in all modes.

ELS_SWP_PWR Opcode: 81 (51 hex)

This command turns the ELS HV power supply on or off. When commanded to turn the ELS power off, the CPU sends command word 6 bit 1 set to 0. When commanded to turn the ELS power on, the CPU sends command word 6 bit 1 set to 1. It always disables sweeping (command word 3 bit 3), sets the sweep length to 1 step (command word 3 bit 2), sets the sweep preset control to 31 (command word 4 bits 4-0), and sets the sweep dE/E control to 3 (command word 3 bits 1-0). This puts the ELS supply in the lowest safe state. The parameters changed by this command are reflected in the following housekeeping parameters: ELS_HV_PWR, ELS_SWP_LEN, ELS_SWP_CTRL, ELS_HV_CTRL, ELS_PSET_ADJ, and ELS_dE_CTRL. This command is valid only in Normal Science. If this command is received in any other mode it is marked as illegal and is ignored. This command is executed immediately upon receipt.

ELS_THRESHOLD Opcode: 150 (96 hex)

This command sets the ELS threshold processing parameters. When the ELS threshold exceeded, ELS is placed in Mode A. This command is valid only in Normal Science. If this command is received in any other mode it is marked as illegal and ignored. This command is executed immediately upon receipt.

5.8.1.7 HVU-1 Commands

The HVU-1 commands are interpreted by CPU 1. These commands are used to turn on/off, safe/arm, enable/disable, and set the high voltage values for the accelerating and retarding supplies. The nominal order of commanding the supplies follows: HVU1_PWR1 (on), HVU1_CNTRL (enable), HVU1_STATE (arm or safe). After this sequence, the HVU1_ACC_ADJ and HVU1_RET_ADJ commands can be used as required. The HVU1_PWR2 command uses a second power switch in the hardware to turn HVU-1 on/off. This command should be used only if the first power switch becomes inactive (broken). See section 4.3.5 and 5548-HVU1 for information on the use and control of the high voltage supplies.

HVU1_ACC_ADJ Opcode: 144 (90 hex)

The HVU1_ACC_ADJ command specifies the Accelerating HV supply voltage DAC level. The Accelerating HV DAC parameter in this command is written to address 40028 hex. The accelerating potential used by CPU 2 is calculated using the equation:

Accelerating Potential = ACC_ADJ * -62.392 / 100.0

The command DAC value is reported in housekeeping by parameter HVU1_ACC_DAC. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the DAC value is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that during normal science operation this command should be selected as a B-cycle boundary command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

HVU1_CNTRL Opcode: 145 (91 hex)

The HVU1_CNTRL command enables or disables the HVU1. Writing any value to 40008 hex enables HVU1. Writing any value to 4000C hex disables HVU1. Execution of this command is reported in housekeeping parameter HVU1_CTRL. Before HVU1 is enabled, the execution of this command sets the DAC values for the Accelerating and Retarding HV supplies to their lowest value as a safety precaution.

This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

HVU1_PWR1 Opcode: 146 (92 hex)

The HVU1_PWR1 command turns the HVU1 power switch 1 on or off. Writing the value 1 to 40030 hex turns power 1 to HVU1 on. Writing the value 1 to 40034 hex turns power 1 to HVU1 off. Execution of this command is reported in housekeeping parameter HVU1_PWR1. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

HVU1_PWR2 Opcode: 147 (93 hex)

The HVU1_PWR2 command turns the HVU1 power switch 2 on or off. Writing the value 2 to 40030 hex turns power 2 to HVU1 on. Writing the value 2 to 40034 hex turns power 2 to HVU1 off. Execution of this command is reported in housekeeping parameter HVU1_PWR2. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

HVU1_RET_ADJ Opcode: 148 (94 hex)

The HVU1_RET_ADJ command specifies the Retarding HV supply voltage DAC level. The Accelerating HV DAC parameter in this command is written to address 4002C hex. The command DAC value is reported in housekeeping by parameter HVU1_RET_DAC. If HVU1 is off or is disabled, this command is marked as illegal and is ignored. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the DAC value is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that during normal science operation this command should be selected as a B-cycle boundary command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

HVU1_STATE Opcode: 149 (95 hex)

The HVU1_STATE command arms or safes the HVU1. HVU1 is safed by (hardware) default after a POR. Writing any value to 40000 hex arms HVU1. Writing any value to 40004 hex safes HVU1. Execution of this command is reported in housekeeping parameter HVU1_STATE. This command executed only if the HVU1 is on. If HVU1 is off, this command is marked as illegal and is ignored. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

5.8.1.8 HVU2 Commands

The HVU2 commands are interpreted by CPU 1. These commands are used to turn on/off, safe/arm, enable/disable, and set the high voltage values for the LEF, ST, and ESA supplies. The nominal order of commanding the supplies follows: HVU2_PWR (on), HVU2_CNTRL (enable), HVU2_STATE (arm or safe). After this sequence, the HVU2_LEF_ADJ, HVU2_ST_ADJ, and HVU2_SWP_CNTRL commands can be used as required. See section 4.3.6 and 5548-HVU2 for information on the use and control of the high voltage supplies.

HVU2_CNTRL Opcode: 152 (98 hex)

The HVU2_CNTRL command enables or disables the HVU2. Writing any value to 40018 hex enables HVU2. Writing any value to 4001C hex disables HVU2. Execution of this command is reported in housekeeping parameter HVU2_CTRL. As a safety precaution, the DAC values for the LEF, ST, and ESA HV supplies are set to their lowest values before HVU2 is enabled. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

HVU2_ESA_ADJ Opcode: 153 (99 hex)

The HVU2_ESA_ADJ command specifies the sweeping HV supply voltage DAC level. The least significant byte of the ESA HV DAC parameter in this command is written to address 38000 hex. The most significant byte of the ESA HV DAC parameter in this command is written to address 38001 hex. The command DAC value is reported in housekeeping by parameters HVU_ESA_DRG and either HVU2_ESA_DAO, HVU2_ESA_DAL, HVU2_ESA_DAM, or HVU2_ESA_DAH, depending on the range bits. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the DAC value is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that this command is used to step the ESA supply "manually" through its range during checkout. Under normal conditions the ESA supply will be swept from the active sweep table following the receipt of an HVU2_SWP_CNTRL command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

HVU2_LEF_ADJ Opcode: 154 (9A hex)

The HVU2_LEF_ADJ command specifies the LEF HV supply DAC voltage level. The LEF HV DAC parameter in this command is written to address 38002 hex. The command DAC value is reported in housekeeping by parameter HVU2_LEF_DAC. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the DAC value is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that during normal science operation this command should be selected as a B-cycle boundary command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

HVU2_PWR Opcode: 155 (9B hex)

The HVU2_PWR command turns the HVU2 power switch on or off. Writing any value to 40038 hex turns power to HVU2 on. Writing any value to 4003C hex turns power to HVU2 off. As a safety precaution, the DAC values for the LEF, ST, and ESA HV supplies are set to their lowest values before HVU2 is turned on. Execution of this command is reported in housekeeping parameter HVU2_PWR. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

HVU2_ST_ADJ Opcode: 156 (9C hex)

The HVU2_ST_ADJ command specifies the ST HV supply DAC voltage level. The ST HV DAC parameter in this command is written to address 38003 hex. The command DAC value is reported in housekeeping by parameter HVU2_ST_DAC. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the DAC value is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that during normal science operation this command should be selected as a B-cycle boundary command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

HVU2_STATE Opcode: 157 (9D hex)

The HVU2_STATE command arms or safes the HVU2. HVU2 is safed by (hardware) default after a POR. Writing any value to 40010 hex arms HVU2. Writing any value to 40014 hex safes HVU2. Execution of this command is reported in housekeeping parameter HVU2_STATE. This command executed only if the HVU2 is on. If HVU2 is off, this command is marked as illegal and is ignored. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

HVU2_SWP_CNTRL Opcode: 158 (9E hex)

The HVU2_SWP_CNTRL command enables or disables the HVU2 ESA sweeping. The control flag is held in CPU 1 memory and does not have a corresponding hardware signal. When enabled, this command allows the active HVU2 ESA sweep table to be used to step the ESA supply. When disabled, the supply is not swept and the lowest voltage value is written to the ESA DAC. When disabled, the HVU2_ESA_ADJ command can be used. Execution of this command is reported in housekeeping parameter HVU2_SW_CTRL. The HVU2 sweep control flag defaults to disable during processor initialization. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the software control flag is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the software control flag is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that during normal science operation this command should be selected as a B-cycle boundary command.

5.8.1.9 IBS Commands

The IBS commands are interpreted by CPU 1. These commands are used to turn on/off, safe/arm, enable/disable, set the high voltage values for the ESA and CEM supplies, enable/disable/configure STIM, set compression strategies and configure ESA sweeping . The nominal order of commanding the supplies follows: IBS_PWR (on), IBS_CNTRL (enable), IBS_STATE (arm or safe). After this sequence, the IBS_CEM_ADJ, IBS_ESA_ADJ and IBS_SWP_CNTRL commands can be used as required. See section 4.3.3 and 5548-IBS for information on the use and control of the high voltage supplies.

IBS_CEM_ADJ Opcode: 104 (68 hex)

The IBS_CEM_ADJ command specifies the CEM HV supply DAC voltage level. The CEM HV DAC parameter in this command is written to address 28002 hex. The command DAC value is reported in housekeeping by parameter IBS_CEM_DAC. This command is valid only in Normal Science mode. If this

command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

IBS_DTM_CNTRL Opcode: 105 (69 hex)

The IBS_DTM_CNTRL enables/disables the dead time correction of IBS sensor data. The dead time correction status is held in a local RAM variable and is reflected in housekeeping by parameter IBS_DTM_CTRL. This command is valid only in Normal Science mode. This command is an implicit A-cycle command. This command is executed on the A-cycle boundary following the receipt of a DPU_A_CYCLE command.

IBS_ESA_ADJ Opcode: 106 (6A hex)

The IBS_ESA_ADJ command specifies the ESA HV supply DAC voltage level. The ESA HV DAC and range parameters in this command are written to address 28000 hex and 28001 hex. The command DAC and range values are reported in housekeeping by parameter IBS_ESA_HV_DAC and IBS_ESA_DAC_RNG. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. This command performs high voltage safety checks before executing the command. If the current voltage is out of tolerance, the command is rejected and the HIGH_VOLTAGE_ERROR bit is set.

IBS_HV_CNTRL Opcode: 107 (6B hex)

The IBS_HV_CNTRL command enables or disables the IBS high voltage supplies. Writing any value to 300E0 hex enables IBS high voltage. Writing any value to 300F0 hex disables IBS high voltage. Execution of this command is reported in housekeeping parameter IBS_CTRL. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

IBS_HV_PWR Opcode: 108 (6C hex)

The IBS_HV_PWR command turns the IBS high voltage power on or off. Writing any value to 300A0 hex turns power to IBS on. Writing any value to 300B0 hex turns power to IBS off. As a safety precaution, the DAC value for the ESA HV supply is set to its lowest values before IBS is turned on. Execution of this command is reported in housekeeping parameter IBS_PWR. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

IBS_HV_STATE Opcode: 109 (6D hex)

The IBS_HV_STATE command arms or safes the IBS ESA supply. IBS is safed by (hardware) default after a POR. Writing any value to 300C0 hex arms IBS. Writing any value to 300D0 hex safes IBS. Execution of this command is reported in housekeeping parameter IBS_STATE. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. This command is executed immediately upon receipt.

IBS_MODE Opcode: 111 (6F hex)

This command is used to set the IBS acqusition strategy between a standard sweep mode (255 energy steps 1 flyback, user defined energy range), solar wind search and track (predefined 255 step search sweep and self-adjusting 127 step monitor sweep) and magnetosphere mode (2 x 255 energy steps providing a 510 step energy range). This command may be executed on either an A-Cycle or B-Cycle boundary and requires an 82DPU_A_CYCLE or 82DPU_B_CYCLE command to execute. This command is valid in all modes.

IBS_STIM **Opcode: 110 (6E hex)**

The IBS_STIM command enables/disables and configures IBS STIM. If stim is being enabled, the channel parameter is written to address 28003 hex bits 8, 9 and10 and the frequency parameter is written to address 28003 hex 12 through 15. If state is enable, a 1 is written to 28003 bit 11. If the state is disable, a 0 is written to 28003 bit 11. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command.

IBS_STIM_TBL **Opcode: 100 (64 hex)**

The IBS_STIM_TBL is used to select one of two internally defined STIM tables and enable/disable IBS STIM. A table number of 1 or 2 will select a STIM table and enable IBS STIM. A STIM table of 0 disables IBS STIM. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command.

IBS_SWP_CNTRL **Opcode: 103 (67 hex)**

The IBS_SWP_CNTRL command enables or disables the IBS ESA sweeping. The control flag is held in CPU 1 memory and does not have a corresponding hardware signal. When enabled, this command allows the active IBS ESA sweep table to be used to step the ESA supply. When disabled, the supply is not swept and the lowest voltage value is written to the ESA DAC. When disabled, the IBS_ESA_ADJ command can be used. Execution of this command is reported in housekeeping parameter IBS_SW_CTRL. The IBS sweep control flag defaults to disable during processor initialization. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the software control flag is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command.

IBS_THRESHOLD **Opcode: 99 (63 hex)**

This command sets the IBS threshold processing parameters. When the IBS threshold is exceeded, the following actions are taken until the count rate is reduced:

Reduce the CEM voltage to 2149 V (dac = 137)
Reduce the CEM voltage to 2102 V (dac = 134)
Reduce the CEM voltage to 2055 V (dac = 131)
Reduce the CEM voltage to 2007 V (dac = 128)
Reduce the CEM voltage to 1898 V (dac = 121)
Finally, ESA and CEM supplies are set to 0.0V and sweeping is stopped.

This command is valid only in Normal Science. If this command is received in any other mode it is marked as illegal and ignored. This command is executed immediately upon receipt.

5.8.1.10 IMS Commands

The IMS commands are interpreted by CPU 1 PROM only. These commands are used to release the IMS cover latch. See section 4.3.8 for a description of the IMS cover latch hardware.

IMS_COV_CNTRL **Opcode: 112 (70 hex)**

The IMS_COV_CNTRL command selects whether the IMS cover release is enabled or disabled. This command is the second command required before the IMS_COVER command can be executed. If IMS cover has not been armed, this command is marked illegal and is ignored. CAPS must be in either the Low Power (ROM) mode or Maintenance mode before this command can be executed, otherwise the command is marked illegal and ignored. This command is executed immediately.

IMS_COV_STATE **Opcode: 113 (71 hex)**

The IMS_COV_STATE command selects whether the IMS cover release is safed or armed. This is the first of two command required before the IMS_COVER command can be executed. CAPS must be in either the Low Power (ROM) mode or Maintenance mode before this command can be executed, otherwise the command is marked illegal and ignored. This command is executed immediately.

IMS_COVER **Opcode: 114 (72 hex)**

The IMS_COVER command releases the IMS cover by activating a WTA (Wax Thermal Actuator). The primary power circuit contains a feedback circuit which will turn the primary power off after cover release. If the primary power circuit fails to release the cover, it must be turned off manually. If primary power fails, the secondary power circuit can be activated with this command. This circuit has no feedback, therefor it must be turned off manually. If the secondary power circuit also fails to activate the WTA, then both the primary and secondary circuits can be turned on. The primary power will be turned off by the activation of the WTA and the secondary power will require manual turn off. If using both power controls fail to activate the WTA, then both must be turned off with this command. The IMS_COV_CNTRL, IMS_COV_STATE commands must be sent before this command is executed, otherwise the command will be marked illegal and ignored. The RT_WTA_ILOCK command must also be sent to enable the wax thermal actuators. CAPS must be in either the Low Power (ROM) mode or Maintenance mode before this command can be executed, otherwise the command is marked illegal and ignored. This command is executed immediately.

IMS_ION_CFG **Opcode: 118 (76)**

This command is used to set the ion data product strategy. This command affects lower telemetry rate data products. When enabled, the first two ions in the data product are always ions 1 and 2 and the third ion cycles between ions 3 to 7 as defined by the ion selection index for the active group table. When disabled the three ions contained in the ion data products will be ions 1, 2 and 3 as defined by the ion selection index for the active group table. This command is an implicit A-Cycle command and requires an 82DPU_A_CYCLE. This command is valid only in normal science mode.

IMS_LOG_SLCT **Opcode: 117 (75)**

This command is used to set the logical data returned in the logicals data product. This command may be executed on either an A-Cycle or B-Cycle boundary and requires and 82DPU_A_CYCLE or 82DPU_B_CYCLE command. This command is valid only in normal science mode.

IMS_SWP_TBL **Opcode: 115 (73 hex)**

The IMS_SWP_TABLE command selects the active HVU-2 ESA sweep table from one of four tables that are available. On POR or reset, table 0 is selected. Presently, only table 0 contains a valid sweep table. The remain tables can be loaded with sweep data using either an ALF load or a Memory Load. This command is valid only in Normal Science mode. If this command is received in any other mode, it is marked as illegal and ignored. If this command's Boundary parameter is IMMEDIATE, it is executed immediately after being received by CPU 1. If the command's Boundary parameter is A_CYCLE, the DAC value is updated on the next A-cycle boundary following the receipt of a DPU_A_CYCLE command. If the Boundary parameter is B_CYCLE, the DAC value is updated on the next B-cycle boundary following a DPU_B_CYCLE command. Both boundary choices require the corresponding DPU_A_CYCLE or DPU_B_CYCLE command. Note that during normal science operation this command should be selected as a B-cycle boundary command.

IMS_THRESHOLD **Opcode: 116 (74 hex)**

This command sets the IMS threshold processing parameters. When the IMS threshold is exceeded, the following actions are taken until the count rate is reduced:

1. Reduce ST supply to 2202 V (dac = 156)
2. Reduce ST supply to 2146 V (dac = 152)
3. Reduce ST supply to 2104 V (dac = 149)
4. Reduce ST supply to 2047 V (dac = 145)
5. Reduce ST supply to 2004 V (dac = 152)
6. Reduce LEF supply to 998 V (dac = 106)
7. Reduce LEF supply to 499V (dac=53)
8. Finally, HVU2 ESA supply sweeping is stopped and the ESA, ST and LEF supplies are set to 0.0V.

This command is valid only in Normal Science. If this command is received in any other mode it is marked as illegal and ignored. This command is executed immediately upon receipt.

5.8.1.11 Memory Commands

The Memory Commands are interpreted by CPU 1 RAM software only. These commands are used to load and patch data tables in memory.

MEM_BLOCK_C **Opcode: 224 (E0 hex)**

The MEM_BLOCK_C command is used to send 1 to 112 words of data to CAPS. This data can be destined for a data table or to patch memory. A large table can be divided into a number of MEM_BLOCK_C commands. The MEM_BLOCK_C commands must be preceded by a MEM_LOAD_C command. This command can be executed in Low Power, Normal Science and Sleep modes. Destinations of CPU 2 requires that CPU 2 is released from reset and executing science software, otherwise the command is marked illegal and ignored. This command is executed immediately.

MEM_BLOCK_NC **Opcode: 225 (E1 hex)**

The MEM_BLOCK_NC command is used to send 1 to 112 words of data to CAPS. This data can be destined for a data table or to patch memory. A large table can be divided into a number of MEM_BLOCK_NC commands. The MEM_BLOCK_NC commands must be preceded by a MEM_LOAD_NC command. This command can be executed in Low Power, Normal Science and Sleep

modes. Destinations of CPU 2 requires that CPU 2 is released from reset and executing science software, otherwise the command is marked illegal and ignored. This command is executed immediately.

MEM_LOAD_C Opcode: 226 (E2 hex)

The MEM_LOAD_C command is used to define a subsequent memory load. It must precede the MEM_BLOCK_C command. This command can be executed in Low Power, Normal Science and Sleep modes. Destinations of CPU 2 requires that CPU 2 is released from reset and executing science software, otherwise the command is marked illegal and ignored. This command is executed immediately.

MEM_LOAD_NC Opcode: 227 (E3 hex)

The MEM_LOAD_NC command is used to define a subsequent memory load. It must precede the MEM_BLOCK_NC command. This command can be executed in Low Power, Normal Science and Sleep modes. Destinations of CPU 2 requires that CPU 2 is released from reset and executing science software, otherwise the command is marked illegal and ignored. This command is executed immediately.

MEM_PATCH_C Opcode: 228 (E4 hex)

The MEM_PATCH_C command is used to send 1 to 112 words of data to CAPS. This data can be destined for a data table or to patch memory. Unlike the MEM_BLOCK_C command, this command can be sent individually and does not require a MEM_LOAD_C command to precede it. This command can be executed in Low Power, Normal Science and Sleep modes. Destinations of CPU 2 requires that CPU 2 is released from reset and executing science software, otherwise the command is marked illegal and ignored. This command is executed immediately.

MEM_PATCH_NC Opcode: 229 (E5 hex)

The MEM_PATCH_NC command is used to send 1 to 112 words of data to CAPS. This data can be destined for a data table or to patch memory. Unlike the MEM_BLOCK_NC command, this command can be sent individually and does not require a MEM_LOAD_NC command to precede it. This command can be executed in Low Power, Normal Science and Sleep modes. Destinations of CPU 2 requires that CPU 2 is released from reset and executing science software, otherwise the command is marked illegal and ignored. This command is executed immediately.

5.8.1.12 Sequence (IEB) Commands

The Sequence commands are interpreted by CPU 1 RAM and PROM software only. These commands are not forwarded on to CPU 2.

SEQ_BLOCK Opcode: 01 (01 hex)

The SEQ_BLOCK command is used to load distributed sequences into CPU 1 memory. From 1 to 112 words of data can be loaded into a distributed sequence. A distributed sequence load can be divided some number of SEQ_BLOCK commands. The data portion of the command contains the actual data table image used by CPU 1 software for distributed sequence processing. A basic distributed sequence command consists of a time tag followed by a command and any command parameters. This command must be preceded by a SEQ_LOAD command. This command is executed immediately.

SEQ_CHECKSUM Opcode: 02 (02 hex)

The SEQ_CHECKSUM command instructs the CPU 1 software to perform an end-around-carry checksum across the specified distributed sequence. The computed checksum is compared with the checksum contained within the command. If the checksums do not match the command is rejected an the Invalid

Command Format housekeeping error bit is set. A distributed sequence checksum must match before a sequence can be executed by the TRIGGER command. This command is executed immediately.

SEQ_END **Opcode: 03 (03 hex)**

The SEQ_END command causes execution of the specified sequence to be halted. A TRIGGER command must be issued again to restart the halted sequence. This command is executed immediately.

SEQ_END_ALL **Opcode: 04 (04 hex)**

The SEQ_END_ALL command causes execution of the all sequences to be halted. A TRIGGER command must be issued again to restart the halted sequences. This command is executed immediately.

SEQ_LINK **Opcode: 05 (05 hex)**

The SEQ_LINK command is used to begin execution of another sequence from within a sequence. It must link to a validated (checksummed) distributed sequences. Otherwise the command is rejected and ignored. This command is executed immediately.

SEQ_LOAD **Opcode: 06 (06 hex)**

The SEQ_LOAD command is used to define a subsequence load of a distributed sequence. It is used to define which sequence will be loaded, the number of SEQ_BLOCK commands to follow and the total number of words that will be transferred. This command is executed immediately.

SEQ_TWEAK **Opcode: 07 (07 hex)**

The SEQ_TWEAK command is used to make minor modifications to already loaded distributed sequence. The sequence is halted if it is an active sequence. The sequence will require a SEQ_CHECKSUM command to verify the sequence before it can be triggered. This command is executed immediately.

TRIGGER **Opcode: 128 (80 hex)**

The TRIGGER command is used to start the execution of a loaded and validated distributed sequence. An error free SEQ_LOAD/SEQ_BLOCK or SEQ_PATCH must have occurred and the distributed sequence must be validated with the SEQ_CHECKSUM command. This command is executed immediately.

5.8.1.13 Miscellaneous Commands

NO_OP **Opcode: 48 (30 hex)**

The NO_OP command is used as a space holder command for distributed sequences. When executing this command, the CAPS software simply verifies the opcode, and increments the command received count and the command executed count. This command is executed immediately.

5.8.2 Instrument Expanded Blocks

CPU 1 is responsible for distributed sequence processing. CPU 1 PROM has five “hard coded” sequence already loaded in PROM. These sequences are:

- Sequence 0 – Actuator Latch Release Power 1
- Sequence 1 – Actuator Latch Release Power 2
- Sequence 2 – IMS cover release power 1
- Sequence 3 – IMS cover release power 2

- Sequence 4 – Actuator Preventative Instrument Maintenance (PIM) sequence

Appendix E lists the commands and timing for these sequences. The distributed sequence are stored as an array of structures. The structure is shown in Table 5.8-1. The location of the sequences is listed in Table 5.8-2.

Table 5.8-2 Structure of a Distributed Sequence

Field	Size	Description
Time Tag	16 bits	The time offset the command is to be executed from last command time.
Command	Variable	This field contains the command opcode and parameters for the command to be executed.

Table 5.8-3 Location of Distributed Sequences

Distributed Sequence	Physical RAM Location (hex)
0	BD000
1	BD400
2	BD800
3-61	BD800 + (IEB – 2) * 64
62	BDF00
63-81	BDF00 + (IEB – 62) * 128
Low Power To Normal Science (82)	BF100
Normal Science To Low Power (83)	BF200
Normal Science To Sleep (84)	BF300
Sleep To Normal Science (85)	BF400
Sleep To Low Power (86)	BF500

All sequences must end with a SEQ_END command.

5.8.3 Interprocessor Commands

CPU 1 and CPU 2 communicate via shared memory and inter-processor commands.

5.8.3.1 Commands Generated By CPU 1

Section 3.2.5.1 describes commands generated by CPU 1. The command is passed to CPU 2 via shared memory and a CPU1-TO-CPU2 interrupt.

5.8.3.2 Commands Processed By CPU 1

Section 3.2.5.1 describes commands generated by CPU 2. CPU 2 passes the commands to CPU 1 via shared memory and a CPU2-TO-CPU1 interrupt. The interrupt handler is responsible for processing the interrupt. The processing associated with each command is described below.

- **B-CYCLE STARTING** – CPU 1 sets a flag to process commands in the B-Cycle queue at the end of the current A-Cycle and increments a B-Cycle counter.
- **PROCESS BACKGROUND** – CPU 1 stops sweeping the ESA supply for one A-Cycle. It also sets the ESA supply to its lowest level.
- **SHARED RAM FAIL** – CPU 1 sets the CPU2 Shared RAM housekeeping bit to indicate the shared RAM test failed

- **SHARED RAM PASS** – CPU 1 sets the CPU2 Shared RAM housekeeping bit to indicate the shared RAM test Passed
- **SAM RAM FAIL** – CPU 1 sets the CPU2 SAM RAM housekeeping bit to indicate the SAM RAM test failed
- **SAM RAM PASS** – CPU 1 sets the CPU2 Shared RAM housekeeping bit to indicate the SAM RAM test Passed
- **RAM FAIL** – CPU 1 sets the CPU2 RAM housekeeping bit to indicate the local RAM test failed
- **RAM PASS** – CPU 1 sets the CPU2 RAM housekeeping bit to indicate the local RAM test Passed
- **THRESHOLD EXCEEDED** – CPU 1 stops sweeping the ESA supply, sets the ESA supply to its lowest level and sets an error bit in housekeeping to indicate the IMS count threshold was exceeded.

5.8.4 Uploads/Patches

Data tables can be updated using ALF, and MEM commands. Uploading new sequences can be done using ALF, MEM and SEQ commands.

5.8.5 PS/RT Commands

The following commands are CAPS commands, but are not processed by CAPS. The PS commands are processed by the SPSS subsystem. The RT commands are processed by the CAPS BIU and not CAPS flight software.

PS_CAPS

This command is directed to the SPSS subsystem and causes CAPS 30V supply to be turned on or off.

PS_HTR

This command is directed to the SPSS subsystem and causes the CAPS replacement heater to be turned on or off.

RT_ARADDR

This command is processed by the CAPS BIU and is used to control the PROM boot address. It sets or clears the BIU discrete bit 3 which is used to change where the boot code phases the ROMmed run-time executable in RAM.

RT_BIU_BIT5

This command is processed by the CAPS BIU and is used to toggle discrete BIT 5 which is unused.

RT_BIU_BIT6

This command is processed by the CAPS BIU and is used to toggle discrete BIT 6 which is unused.

RT_BIU_BIT7

This command is processed by the CAPS BIU and is used to toggle discrete BIT 7 which is unused.

RT_OPMODE

This command is processed by the CAPS BIU and defines discrete command bits 1 and 2. These bits form a H/W interlock value for CAPS software. When the bits value is cleared (set to 00) or set to binary 10, CAPS software must stay in the SLEEP state. When the bits are set to binary 01, then CAPS is permitted to perform science operations without articulation. When the bits are set to binary 11, then CAPS is permitted to perform science operations with articulation (the actuator is allowed to move).

RT_RESET

This command is processed by the CAPS BIU and defines discrete command bit 0 as the CAPS hardware subsystem reset. When this bit is set, the CAPS subsystem will be held in reset. When this bit is cleared, the CAPS subsystem is released from reset. This discrete bit is tied directly to the system reset.

RT_WDTERR_CAPS

This command is processed by the CAPS BIU and is used to clear the BIU watchdog timer expired flag in the CAPS BIU. Once this flag has been cleared, the CAPS BIU will be able to communicate with the ‘prime’ CDS if the failure to communicate was due to a watchdog expiration event.

RT_WPERR_CAPS

This command is processed by the CAPS BIU and is used to clear the BIU write protection violation flag which has been set due to the faulty operation of the BIU. Setting this bit will simulate the occurrence of a write protect violation.

RT_WPFNC_CAPS

This command is processed by the CAPS BIU and is used to enable or disable the write protect function of the CAPS BIU which protects the auto-initialization table in a BIU. Once the write protect function is disabled, the CDS may write into the auto-init table of the CAPS BIU. Write protection is usually enabled and prevents the auto-initialization table from being corrupted.

RT_WTA_ILOCK

This command is processed by the CAPS BIU and is used to set or reset the BIU discrete command bit 4 which is the wax thermal actuator interlock bit. This bit must be set for either the ACT_LATCH or IMS_COVER commands to function.

5.9 MIL-STD-1750A Microprocessor

CPU 1, CPU 2 and SAM microprocessors are PACE 1750As utilizing an 8 MHz system clock. The MIL-STD-1750A microprocessor is a 16-bit processor with 32 bit and 48 bit floating point arithmetic. The 1750A has two companion chips PACE 1753 Memory Management Unit (MMU) and PACE 1754 Processor Interface Circuit (PIC). The 1750A microprocessor is a 16 bit machine. All operations are on 16-bit word boundaries. By using the 1753 MMU, CAPS has a one megaword address space. (see section 4.2 for a map of CPU 1 memory). Bit 0 is the most significant bit of a word. The 1750A word format is shown in Figure 5.9-1.

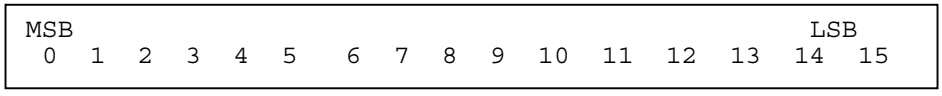


Figure 5.9-1 1750A Word Format

5.9.1 1750A Registers

The 1750A has 24 user-accessible registers:

- 16 General Purpose Registers designated R0-R15
- Pending Interrupt Register – The 1750A has seven internal and nine external interrupts. These interrupts are latched in the appropriate bit in the Pending Interrupt Register.
- Mask Register – The Mask Register is used to disable selected interrupts.
- Fault Register – This register is a 16-bit register which saves fault information.
- Status Word Register – This register is a 16-bit register that can be modified under program control. It contains program flags (carry, positive, zero and negative), access key, and address state.
- Instruction Counter – This register is the pointer to the next instruction to execute.
- System Configuration Register – This register contains five bits which identify the configuration of the external system being used with the 1750A processor.
- Timer A – One of two internal timers. This timer runs off a 100 kHz clock.
- Timer B – The second of two internal timers. This timer runs off a 10 kHz clock.

See the PACE1750A documentation or MIL-STD-1750a for more information on the 1750A registers.

5.9.2 Processor Interface Circuit

The PACE 1754 provides the following system functions:

- Programmable system watchdog.
- Programmable READY generation
- Automatic READY generation
- Timer Clock Generation used by the 1750a TIMERA and TIMERB

The CPU1 software configures the PIC registers as follows:

Control Register – The value 0000 is written to this register.
Memory Ready Program Register – The value 1201 hex is written to this register
I/O Ready Program Register – The hardware default is used.
Program Register – The value 4000 hex is written to this register. It is also used to enable/disable the watch dog timer.
Watch Dog Timer Register – This register is initialized with 0000 and later the value 7EF4 hex.
Unimplemented Memory register – The hardware default is used.
First Unimplemented Output Command – The hardware default is used.
First Unimplemented Input Command – The hardware default is used.
Register Failing Address – The hardware default is used.

See the PACE1750A documentation or MIL-STD-1750a for more information on the 1754 registers.

5.9.3 Memory Management Unit

The PACE 1753 provides memory management capabilities for the system. A physical address is 20 bits wide. The 1750A microprocessor is limited to a 16 bit address or a 64k address space. This is called the logical address. To get around the 64k limitation, the MMU is used to extend the 16 bit address to 20 bits.

The MMU provides up to 256 blocks of 4k words of instruction and data space (effectively 2 megawords of configurable address space). There are 16 memory pages with each page containing 16 page registers. A memory page can address 64k of address space. The Address State field in the 1750A Status Word register is used to select

one of the 16 memory pages. The most significant nibble (bits 0-3) is used to select one of 16 page registers in the selected memory page. Each page register contains 16 bits of information. The most significant nibble (bits 0-3) is an access key. Each page register can access a four kword block of memory. The lower 12 bits of the logical address are concatenated to the 8 (bits 8-15) bits in the page register to form the 20 bit physical address. This address is then strobed onto the address bus to select a specific memory cell. The MMU contains nine control registers. They are configured as follows.

- **Control Register** – The hardware default is used.
- **Control Register 1** – The hardware default is used.
- **Unimplemented Memory Register 1** – The hardware default is used.
- **Unimplemented Memory Register 2 –**The hardware default is used.
- **First unimplemented Output Command** – The hardware default is used.
- **First unimplemented Input Command** – The hardware default is used.
- **First Failing Address Register** – The hardware default is used.
- **First Failing Data Register** – The hardware default is used.
- **Memory Fault Status Register** - The hardware default is used.

See the PACE1750A documentation or MIL-STD-1750a for more information on the 1753 registers.

5.9.4 Jump Tables and Context Switches

Since CAPS has a one megaword address space and the 1750a has a 64k address space limitation, it is necessary to manipulate the 1753 to map in the required code and data. The 1750A contains a program status word register. As described in the previous paragraph, this register is used in conjunction with the 1753 to produce the 20-bit address . The status word register address state field is updated when a context switch occurs. A context switch occurs when an interrupt occurs or a LST (Load Status) instruction is executed. The LST instruction contains a pointer to a structure containing the new interrupt mask, new status word register (containing a new address state), and instruction counter. This process is referred to as a long call. The design for a long call procedure is:

```
Type LONG_CALL_STRUCTURE is
        Record
                Unsigned 16bit integer IRQ_MASK;
                Unsigned 16bit integer STATUS_REGISTER_MASK;
                Unsigned 16bit integer INSTRUCTION_COUNTER;
                Unsigned 16bit integer SAVED_R0;
        End record

Type RETURN_STRUCTURE is
        Record
                Unsigned 16bit integer IRQ_MASK;
                Unsigned 16bit integer STATUS_REGISTER_MASK;
                Unsigned 16bit integer INSTRUCTION_COUNTER;
        End record

THE_JUMP_TABLE is array (all procedures that require long calls) of LONG_CALL_STRUCTURE
THE_RETURN_TABLE is array (all procedures that require long calls) of RETURN_STRUCTURE

procedure GENERIC_LONG_CALL is
BEGIN
        save the return address
        get the mask register and save it for the new procedure and the return back
        Use the LST instruction to call the entry routine from THE_JUMP_TABLE using
        LONG_CALL_STRUCTURE
        -- the called routine will return immediately following the LST instruction
<GENERIC_RET>
        return to the calling function
END

Procedure GENERIC_LONG_CALL_ENTRY is
BEGIN
        Call the function
        Use the LST instruction to return to <GENERIC_RET> from THE_RETURN_TABLE using
        RETURN_STRUCTURE
END
```

These procedures and tables are implemented in assembly language.

APPENDIX A: Acronyms

A

AHVPS - Accelerating High Voltage Power Supply
ACT - Actuator
ADC - Analog to Digital Converter
ATLO - Assembly Test and Launch Operations
ATP - Acceptance Test Plan

B

BIT - Built In Test
BIU - Bus Interface Unit
BIUFR - Bus Interface Unit Functional Requirements Document
BIUHSI - Bus Interface Unit Hardware/Software Interface Document

C

CAPS - Cassini Plasma Spectrometer
CAR - Corrective Action Request
CASE - Computer Aided Software Engineering
CDR - Critical Design Review
CDS - Command and Data System
CEM - Channeltron Electron Multiplier
CFS - Cassini Flight Software
CMP - Cassini Mission Plan
Co-I - Co-Investigator
CPU - Central Processing Unit

D

DAC - Digital to Analog Converter
DE - Direct Events
DPU - Data Processing Unit
DT - Dead Time
DTSTART - Dead Time Start

E

EGSE - Electronic Ground Support Equipment
EL - Elevation
ELS - Electron Spectrometer
EM - Engineering Model
EMI - Electromagnetic Interference
E/Q - Particle Energy/Charge
ESA - Electrostatic Analyzer

F

FEE - Front End Electronics
FIFO - First-In First-Out
FOV - Field Of View
FPP - Fields and Particles Pallet
FSDD - Flight Software Detailed Design
FSFD - Flight Software Functional Design

FSRD - Flight Software Requirements Document
FSSRD - Flight Software Science Requirements Document

G

GS - Ground System
GSFC - Goddard Space Flight Center

H

HK - Housekeeping
HV - High Voltage
HVPS - High Voltage Power Supply
HVU1 - High Voltage Unit 1
HVU2 - High Voltage Unit 2

I

IBS - Ion Beam Spectrometer
ICD - Interface Control Document
IDD - Instrument Description Document
I/F - Interface
IMS - Ion Mass Spectrometer
I/O - Input/Output

J

JPL - Jet Propulsion Laboratory

K

kbps - kilo bits per second

L

LAM - Latch Actuating Mechanism
LEF - Linear Electric Field
LOG - Logic
LVPS - Low Voltage Power Supply

M

MCP - Microchannel Plate
M/Q - Mass/Charge
MRO - Memory Readout

N

NR - Nonconformance Report

O

OP - Operating Procedure

P

PI - Principal Investigator
PM - Project Manager
POR - Power On Reset
PP&R - Project Policies and Requirements Document
PROM - Programmable Read Only Memory

Q

QA - Quality Assurance
QAP - Quality Assurance Procedure

R

RAM - Random Access Memory
RHVPS - Retard High Voltage Power Supply
ROM - Read Only Memory
RTI - Real Time Interrupt

S

SAM - Spectrum Analyzer Module
S/C - Space Craft
SDF - Software Development Folder
SING - Singles
SMU - Sensor Management Unit
SPCR - Software Problem/Change Report
SSR - Solid State Recorder
SwRI - Southwest Research Institute

T

TBD - To Be Determined
TDC - Time to Digital Converter
TLM, TM - Telemetry
TOF - Time of Flight
TRR - Test Readiness Review

U-W

WIP - Work Implementation Plan
WTA - Wax Thermal Actuator

X-Z

ZLP - Zero Length Packets

APPENDIX B: Requirements Traceability Matrix

This appendix contains the Requirements Traceablility Matrix. This matrix first appears in 5548-FSRD-01, the Cassini/CAPS Flight Software Requirements Document. The matrix has been modified for this document. Columns have been added to show where a requirement is met by the design presented in this FSFD documented.

TBD and updated...

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.1.1-1	CAS-3-310	68223	CCSDS Recommendation for Space Data System Standards, Time Code Formats
r3.1.2-1	5548-FSSRD:3.3	-	CAPS system time synchronized to S/C 64 seconds
r3.1.2-2	5548-FSSRD:4.1.1	-	Sample times: IMS-62.50 ms; ELS-31.25 ms; IBS-7.8125 ms
r3.1.2-3	5548-FSSRD:4.1.1	-	DPU sample clock can be changed on command to lengthen sample intervals by x2, x4, or x8
r3.1.2-4	5548-FSSRD:4.1.1	-	512 second B-cycle option
r3.1.3-1	5548-FSSRD:5.1.4	-	Submodes CAL_SCI and CAL_ENG shall be provided within Mode 0
g3.1.3-1	5548-FSSRD:5.1.4	-	CAL_SCI to demonstrate end-to-end system level performance of all sensors as well as internal data handling
r3.1.3-2	5548-FSSRD:5.1.4	-	CAL_ENG shall test all engineering functions of DPU and sensors
r3.1.3-3	5548-FSSRD:6.3.1	-	Other modes/submodes can be added to Mode 0; Mode 0 modifiable
r3.2-1	CAS-3-310:4.3.2.1-4	67730	All bus users shall use BIU, XBA, or REU
r3.2-2	CAS-3-310:4.3.2.1-4	67730	CFS shall use BIU
r3.2-3	CAS-3-310:3.3.2.1-5	67731	BIU shall support interfaces a) thru g) as listed
r3.2-4	CAS-3-310:4.3.2.2-4	67741	BIU shall not support Mode Code 0, Select Xmitter shutdown, Override Selected Xmitter Shutdown
r3.2-5	CAS-3-310:4.3.2.2-5	67742	Bus users shall illegalize all illegal, reserved, and unimplemented mode codes
r3.2-6	CAS-3-310:4.3.2.2-7	67744	Optional BIU subaddresses not used by instrument shall be illegalized by that system
r3.2-7	CAS-3-310:4.3.2.2-9	67748	Instr. shall configure BIU to respond correctly to CDS initiated collections of user data
r3.2-8	CAS-3-310:4.3.3-2	67752	Processor-assisted instruments shall support listed subset of total communications services
c3.2.1-1	BIUFR:4.2-5	BIU 056	During auto-initialization the host shall be precluded from accessing BIU RAM or registers
c3.2.1-2	BIUFR:4.2-6	BIU 057	The host shall be precluded from altering the first 320 words of BIU RAM
r3.2.1-1	BIUFR:4.4-1	BIU 068	9 discrete statuses from the host are supported; 8 user defined, 1 subsystem fail status
c3.2.1-3	BIUFR:5.0-11	BIU 100	The user shall not attempt to write to the lower BIU auto-initialization table
r3.2.1-2	BIUFR:5.0-12	BIU 101	The user shall illegalize the dynamic bus control mode code within any user generated RT Descriptor tables

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	Requirement Source	Project Req.	Description
c3.2.1-4	BIUFR:5.0-13	BIU 102	Users are prohibited from redefining preassigned Remote Terminal Descriptor table entries
c3.2.1-5	BIUFR:5.0-20	BIU 109	User software shall not write to BIU registers R1, R3, R5, R14, R15, R16, and R17
c3.2.1-6	BIUFR:5.0-21	BIU 110	User software shall only modify BIU registers during the bus dead time period (after DTSTART)
r3.2.1-3	BIUFR:5.0-22	BIU 111	Users shall be self safing when communications with CDS lost for longer than watchdog time-out interval
r3.2.1-4	BIUHSI:3.7.3	-	BIU hosts are expected to be tolerant of RTI and DTSTART drop outs for several seconds
r3.2.1-5	CAS-3-310	ECRC 80243	Instruments shall use a pattern of one or more discretes as Power Discrete (internal operating state) interlock
r3.2.1-6	CAS-3-310	ECRC 80243	Power discretes shall be defined so that low (zero or all zeros) corresponds to the sleep state
r3.2.1-7	CAS-3-310	ECRC 80243	Instrument shall implement their response to BIU power discretes so that the response is programmable in flight
r3.3-1	CAS-3-310:4.3.3.1-4	67768	The maximum bus command length shall not exceed 128 words
r3.3-2	CAS-3-310:4.3.3.1-6	67770	Instruments shall be able to receive commands of the listed (a-d) types
r3.3-3	CAS-3-310:4.3.3.1-7	67772	Receipt of conflicting commands will give end state precedence to the highest priority command
r3.3-4	CAS-3-310:3.3.2.2-1	68175	Commands that have 2 or more independent variables shall have no change as a valid parameter value for each
r3.3.1-1	5548-FSRD Design	-	CAPS shall provide commands which allow increasing/decreasing the DPU and SAM processor rates
r3.3.2-1	5548-FSSRD:4.2	-	CAPS commands shall be divided into Critical, Engineering, and Science categories
r3.3.2-2	5548-FSSRD:4.1.2	-	Each CAPS command description shall indicate whether it is critical or takes place on A- or B-cycle boundaries

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.3.2-3	5548-FSSRD:4.3	-	Command execution by CAPS shall allow the one of four listed options independently of each other
r3.3.2-4	5548-FSSRD:4.1.2	-	CFS shall not execute a second command of the same type as a pending command
r3.3.3-1	CAS-3-310:3.3.2.2.2-5	68183	Science instruments shall be primarily operated in flight through on-board stored sequences
r3.3.3-2	CAS-3-310:4.2.2.6-1	30494	Instruments shall provide a means of ground verification of distributed sequence loads
r3.3.3-3	CAS-3-310:4.2.2.6-2	30495	Instruments shall provide a means for sequence tweaking
r3.3.3-4	5548-FSSRD:4.1.2	-	CFS shall not exclude the use of sensor-specific command modules
r3.3.4-1	CAS-3-310:3.2.2.2-2	68179	Computer-based instruments with RAM memory shall accommodate new program loads via uplink command
r3.4-1	CAS-3-310:xxxx	68195	Instruments shall form telemetry data into two types of packets: housekeeping data and science data
r3.4.1-1	CAS3.310:4.4.2.2.2-3	67928	Telemetry packet producer shall respond to pending mode change with correct packet size/rate
r3.4.1-2	CAS-3-310:4.4.3.1.1-2	67968	Telemetry packet collection rate allocation shall include CCSDS packetization overhead as part of rate
r3.4.1-3	CAS-3-310:4.4.3.1.1-5	67972	Within a S/C mode, packet size and pickup rate shall remain constant for a single packet production source
r3.4.1-4	CAS-3-310:4.4.3.1.1-4	67971	Packet collection repeat cycle shall be expressible in 2^n seconds where n is a non-negative integer ≤ 9
r3.4.2-1	CAS-3-310:4.4.2.2.1-5	67920	Changes to telemetry data production rate within a S/C telemetry mode shall be invisible to S/C telemetry mode
r3.4.2-2	CAS-3-310:4.4.2.3-15	67957	Sources producing telemetry data at a rate lower than S/C telemetry mode shall provide zero length packets
r3.4.2-3	5548-FSSRD:3.3	-	CFS shall allow management of data volume via choice of operating modes and data compression strategy
r3.4.3-1	CAS-3-310:4.4.2.3-1	67937	Instruments on board the S/C shall packetize their internally generated telemetry data in CCSDS TLM packets
r3.4.3-2	CAS-3-310:4.4.2.3-2	67938	CCSDS telemetry packets shall always be an even integer number of octets in length
r3.4.3-3	CAS-3-310:4.4.2.3-3	67939	The maximum science packet length, including packet header, shall not exceed 8720 bits
r3.4.3-4	CAS-3-310:4.4.2.3-4	67941	TLM packet producers shall identify packet data format and contents via the primary header app. process id

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.4.3-5	5548-FSRD Design	-	CAPS shall not use mini-packets in its science or housekeeping telemetry streams
r3.4.3-6	5548-FSRD Design	-	The time stamp of successive packets shall be linearly increasing
r3.4.3-7	CAS-3-310:4.4.2.3-6	67944	All telemetry packets shall contain a time stamp field consisting of 40 bits of S/C time
r3.4.3-8	CAS-3-310:4.4.2.3-7	67945	A producer of telemetry packets shall time stamp the packets prior to their collection by the CDS
r3.4.3-9	CAS-3-310:4.4.2.3-8	67946	Telemetry packets shall contain a packet collection error flag field which will be set by CDS if bus errors
r3.4.3-10	CAS-3-310:4.4.2.3-9	67947	Each packet source shall set the packet error collection field to zero
r3.4.4-1	CAS-3-310:4.4.2.3-10	67950	Science housekeeping packet size per source shall be fixed throughout the mission
r3.4.4-2	CAS-3-310:4.4.2.3-11	67951	Science housekeeping packet size shall not exceed 100 words
r3.4.6-1	CAS-3-310:4.4.2.3-15	67959	The packet sequence count field in the second word of TLM packet header shall not be incremented for ZLPs
r3.5-1	5548-FSSRD:6.2.2	-	During HV operation, the CFS shall limit check detector count rates as well as a set of HK parameters
r3.5-2	5548-FSSRD:6.2.2	-	It shall be possible to upload new detector limits/countermand limit exceeded logic of limit checking function
r3.5-3	5548-FSSRD:6.3.10	-	If the test history of CAPS warrants, the CFS shall be able to react to out-of-limits data by listed (1-3) options
r3.5-4	5548-FSSRD:6.3.10	-	In the event that CAPS safes its HV supplies, it shall be possible to override the safing
r3.5.1-1	5548-IBS:3.1.3.3	-	CFS shall address the CEM DAC register, the ESA buffer register, and the stim register
r3.5.1-2	5548-IBS:3.1.3.2	-	The CFS shall issue commands to the IBS sensor over a bi-directional 8 bit command interface
r3.5.1.1-1	5548-IBS:3.1.2.1	-	The CEM PS shall be under control of the CFS and shall be 8-bit programmable from 0 to -4.0kV
r3.5.1.2-1	5548-IBS:3.1.2.2	-	The ESA PS output voltage shall be controlled from the CFS by writing 2 8-bit data words to the IBS data latch
r3.5.1.2-2	5548-IBS:3.1.3.5	-	The ESA voltage shall be commanded to the level desired for the next acquisition period
r3.5.1.3-1	5548-IBS:3.1.3.8	-	The stim function shall be controlled by the CFS by writing an 8-bit control word to the stim register

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.5.2-1	5548-ELS:3.1.3.3	-	The CFS shall issue commands to the ELS sensor over a one way, 8-bit command interface
r3.5.2.-2	5548-ELS:3.1.3.3	-	A sweep command requires both Addr 3 and 4 commands are updated (3 before 4)
r3.5.2-3	5548-ELS:3.1.3.3	-	MCP HV command requires Addr 2 and 6 commands be updated within 100 µsec
r3.5.2.1-1	5548-ELS:3.1.2.1	-	The CFS shall control the ELS MCP power generator via a 5-bit control bus
r3.5.2.2-1	5548-ELS:3.1.2.2	-	The CFS shall control the selection of the ELS stepping voltage generator sweep table
r3.5.2.3-1	5548-ELS:3.1.2.3	-	The CFS shall control the HV enable to the HV power supplies
r3.5.2.4-1	5548-ELS:3.1.3.3.1	-	The SMU stim pulse generator shall be enabled and disabled by command from the CFS
r3.5.2.4-2	5548-ELS:3.1.3.3.1.1	-	The SMU srim pulse generator variable amplitude mode shall be selected by command
r3.5.2.4-3	5548-ELS:3.1.3.3.1.1	-	The SMU stim pulse generator constant amplitude mode shall be selected by command
r3.5.3-1	5548-TDC:3.2	-	The DPU shall configure the TDC and read the singles counters from the TDC
c3.5.3-1	5548-TDC:3.2.4.7	-	The DPU should not write FEE config registers when their contents are being transmitted to the FEE
r3.5.3.1-1	5548-IMS:3.1.2.1	-	RHVPS control shall be via an 8-bit DAC covering range 0 to +16kV (operate at +8kV to +16kV)
r3.5.3.2-1	5548-IMS:3.1.2.2	-	AHVPS control shall be via an 8-bit DAC covering range 0 to -16kV (operate at -8kV to -16kV)
r3.5.3.3-1	5548-IMS:3.1.2.5	-	Stepping PS control via 2-bit range and 12-bit DAC covering 1eV to 50keV (-0.16 V to -7415 V)
r3.5.3.4-1	5548-IMS:3.1.3.4	-	IMS BIT frequency and delay shall be set by the DPU
r3.5.3.5-1	5548-IMS:3.1.3.5	-	Timing discriminator thresholds shall be changable to one of 15 higher levels by DPU command
r3.5.5-1	5548-FSSRD:3.3	-	ACT operation (on/off) shall be synchronized with the S/C master frame time interval of 64 seconds
r3.5.5-2	5548-FSSRD:4.1.1	-	ACT timing shall not be synchronized with A or B cycles
r3.5.5.-3	5548-ACT:3.3.7	-	ACT control is via two 8-bit control words at a fixed rate of once per 7.81250 msec

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.5.2-1	5548-ACT:3.1.2	-	Subsets of the 208° normal range of motion (e.g. ±32°) shall also be programmable
r3.5.2-2	5548-FSSRD:6.3.8	-	It shall be possible to dither teh ACT for to point it in a given direction
r3.5.2-3	5548-FSSRD:6.3.8	-	In the event that ACT is allowed to operate only for short periods, CFS shall move ACT and then halt
out	5548-IBS:3.1.3.7	-	The CFS shall be able to vary the IBS step time from 1/8, 1/4, 1/2, to 1/1 of basic CAPS step time
r3.6.1.1-1	CAS-3-310:4.3.3.4-3	67792	The time broadcast message shall indicate the S/C time at the next RTI plus one
r3.6.1.3-1	CAS-3-310:xxxx	67841	CAPS shall receive: thruster warning, S/C attitude, and MAG instantaneous filed vector ancillary data
r3.6.1.3-2	5548-FSRD Design	-	CAPS shall also receive the RPWS Sounder operation and Langmuir Probe bias potential data
r3.6.2-1	CAS-3-310:xxxx	67952	When an instrument is on, it shall always produce valid science HK packets at the rate CDS collects them
r3.6.2-2	CAS-3-310:4.4.2.1-16	67896	Science housekeeping packets shall contain health, safety, and status data
r3.6.2-3	CAS-3-310:3.3.3.2-1	68190	Instruments shall not include on-board generated data in their housekeeping packets if available on ground
r3.6.2-4	5548-FSSRD:6.1	-	Initial checkout, IMS cover and ACT latch release, and ACT maint. shall rely only on HK for reporting
r3.6.2-5	CAS-3-310:4.4.2.1-14	67892	Instruments shall provide number of commands received, rejected, and executed in HK stream
g3.6.2-1	CAS-3-310:4.4.2.1	-	CAPS should include operation code (op code) of the last received command in HK packets
r3.6.2-6	5548-FSRD Design	-	CAPS shall collect and format HK monitors, statuses, and values as described in 5548-FSFD-01
r3.6.2-7	5548-FSSRD:6.1.4	-	Monitoring of the ACT maintenance operation shall be possible through HK data steam only
r3.6.2-8	5548-FSRD Design	-	HK packets shall include (TBD) number of bytes for trickled MRO; start addresses chosen by command
r3.6.3.1-1	5548-FSSRD:6.3.3	-	The CFS shall acquire 3 16-bit EL values per 7.8125 ms acquisition period
r3.6.3.1-2	5548-IBS:3.1.3.1	-	The IBS counters shall be read and reset by the CFS after each accumulation period
r3.6.3.2-1	5548-FSSRD:6.3.3	-	The CFS shall acquire 8 16-bit EL values per 31.25 ms acquisition period

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.6.3.2-2	5548-ELS:3.1.3.2	-	The CFS shall read and report the ELS counter data
r3.6.3.4-1	5548-FSSRD:6.3.3	-	The CFS shall acquire 8 16-bit EL and 4 16-bit LOG values from TDC every 62.50ms period
r3.6.3.3-2	5548-FSSRD:6.3.3	-	The CFS shall acquire 512 32-bit TOF values from SAM every 62.50 ms acquisition period
r3.6.3.4-1	5548-FSSRD:6.3.5	-	During one A-cycle out of every N (commandable), E/Q steps are set to 0 (background measurement)
r3.7.1-1	5548-FSSRD:6.3.4	-	All data used in any on-board calculation shall be dead time corrected prior to the calculation
r3.7.1-2	5548-FSSRD:6.3.4	-	Dead time correction shall be enabled or disabled by command
r3.7.1-3	5548-FSRD Design	-	The DT enable/disable commands shall allow enable/disable of calculation on a per instrument basis
r3.7.1-4	5548-FSRD Design	-	Dead time correction shall be enabled for all sensors by default
r3.7.2-1	5548-FSSRD:6.3.7	-	The CFS shall send a M/Q list to SAM; command selectable; minor species rotated within the list
r3.7.2-2	5548-FSSRD:4.1.2	-	The ION identifiers selected from IMS M/Q tables shall be encoded in IMS data product
r3.7.3-1	5548-FSSRD:6.3.12	-	Prior to formatting for telemetry, data shall be log compressed (16 $\rightarrow$ 8 or 32 $\rightarrow$ 16 bits) per data word
r3.7.3-2	5548-FSSRD:6.3.12	-	The compression (decimation) schemes shown in FSSRD Table 6.3.12-2 shall be active automatically by mode
r3.7.4-1	5548-FSSRD:6.3.12	-	The listed data product types shall be produced by the CFS
r3.6.4-1	CAS-3-310:4.4.2.1-18	67901	If an instrument is commanded to produce a MRO, this data shall be included in its telemetry packet(s)
r3.8-1	5548-FSSRD:5.1.6	-	CFS shall provide a MRO capability dumping DPU and SAM instead of performing computations, etc
r3.8-2	5548-FSSRD:5.1.6	-	The MRO mode shall allow readout of TOF DE data.
r3.9.1-1	5548-FSRD Design	-	CFS shall verify proper hardware operation and initialize the system to a know default state
r3.9.1.1-1	5548-FSRD Design	-	RAM tests shall be performed by the CFS in the two CPUs on their respective memories
r3.9.1.1-2	5548-FSRD Design	-	The success or failure status of the RAM tests shall be reported in the housekeeping telemetry data

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
r3.9.1.2-1	5548-FSRD Design	-	The two CFS processors shall each calculate a checksum over their respective PROM space
r3.9.1.2-2	5548-FSRD Design	-	The status of the PROM checksum comparisons shall be reported in the HK telemetry data
r3.9.3.1-1	5548-FSSRD:3.3	-	All SAM flight code shall be stored in the SSR and shall be downloaded by the CFS during SAM initialization
r4.1-1	CAS-3-310:4.2.2.2-8	67669	The time at which CFS begins execution of a command shall be predictable to within 1 second
r4.1-2	CAS-3-310:4.2.2.2-9	67670	The time at which a CFS command completes shall be a boundable, finite amount of predictable time
r4.1-3	5548-ELS:3.1.3.4	-	Time between two successive ELS commands must be ≥ 1μs
r4.2-1	5548-ELS:6.3.2	-	The CFS shall perform each sensor PS stepping function independently; simultaneously with respect to time
r4.2-2	5548-FSSRD:5.1.3	-	The CFS shall provide for separate and stepwise activation of all CAPS sensor high voltages
r4.3-1	5548-FSSRD:5.1.2	-	A special high-speed data rate mode of 24 kbps shall read out data 8 times faster for ground testing
r4.4-1	CAS-3-310:ECRC 80243	-	Instruments will check and respond to power discretes, if required, within 10 seconds of discrete changing state
r5.0-1	5548-FSSRD:5.1	-	The CFS shall function with one, two, or three sensors in operation (sensors can operate independently)
r5.0-2	CAS-3-310:4.3.3.3-1	67785	All bus users shall provide discrete status to the CDS on request
r6.0-1	5548-FSSRD:3.3	-	Except boot-up code stored in CAPS PROM, all CFS will be stored in the SSR and downloaded on command
r6.0-2	5548-FSSRD:6.3.1	-	Mode 0 shall be designed such that other modes/sub-modes can be added post launch; patching provided
g6.0-1	5548-FSSRD:4.1.2	-	It is a goal for the CFS system to contain 2 AMx tables for IMS; 2 ABx tables for IBS
r6.0-3	5548-FSSRD:4.1.2	-	ION selection for the IMS shall require 16 M/Q tables
g6.0-2	5548-FSSRD:4.1.2	-	It is a goal to have 4 B-tables resident in memory for each sensor
r6.0-4	5548-FSSRD:4.4	-	CFS shall be compatible with PD 699-110 with respect to the number and size stored in CDS and uplinked
r6.0-5	5548-FSSRD:4.4	-	CAPS shall be able to be commanded to switch operating modes twice/day with max 6/day

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**
g6.0-3	5548-FSSRD:5.1.1	-	Goal that all ground tests and operations software be the same as flight software
r6.0-6	5548-FSSRD:5.1.5	-	Stim pulses can be chosen by varying pulser rate as a function; several TOF values stim'd
r7.1-1	PP&R:2.3-4	1840	Ada is recommended for instruments which use 1750A processor
r7.1-2	WIP:xxxx	-	CFS shall be written using the Ada programming language
g7.2-1	WIP:xxxx	-	CFS will be developed using the CADRE CASE tool
g7.2-2	WIP:xxxx	-	CFS will be unit tested using the C-TAC imulator

REQUIREMENTS TRACEABILITY MATRIX

CAPS Req.	**Requirement Source**	Project Req.	**Description**

APPENDIX C: Compression Encoding

This Appendix contains the 16-bit to 8-bit compression table. This table is used by the Cassini/CAPS flight software to compress 16-bit sensor science data.

LOSSY COMPRESSION ENCODING (16→8 Bits)

Input Range (Min)	**Code**	**Input Range** (Min)	**Code**	**Input Range** (Min)	**Code**	**Input Range** (Min)	**Code**
0	0	21	21	43	42	92	63
1	1	22	22	45	43	95	64
2	2	23	23	47	44	98	65
3	3	24	24	49	45	101	66
4	4	25	25	51	46	105	67
5	5	26	26	53	47	109	68
6	6	27	27	55	48	113	69
7	7	28	28	57	49	117	70
8	8	29	29	59	50	121	71
9	9	30	30	61	51	125	72
10	10	31	31	63	52	129	73
11	11	32	32	65	53	133	74
12	12	33	33	67	54	138	75
13	13	34	34	69	55	143	76
14	14	35	35	71	56	148	77
15	15	36	36	74	57	153	78
16	16	37	37	77	58	158	79
17	17	38	38	80	59	164	80
18	18	39	39	83	60	170	81
19	19	40	40	86	61	176	82
20	20	41	41	89	62	182	83

188	84	398	106	844	128	1787	150
194	85	412	107	873	129	1849	151
201	86	427	108	903	130	1913	152
208	87	442	109	934	131	1979	153
215	88	457	110	966	132	2048	154
223	89	473	111	1000	133	2112	155
231	90	489	112	1035	134	2176	156
239	91	506	113	1071	135	2240	157
247	92	524	114	1108	136	2304	158
256	93	542	115	1147	137	2400	159
265	94	561	116	1187	138	2496	160
274	95	580	117	1228	139	2592	161
283	96	600	118	1271	140	2688	162
293	97	621	119	1315	141	2784	163
303	98	643	120	1360	142	2880	164
314	99	665	121	1407	143	2976	165
325	100	688	122	1456	144	3072	166
336	101	712	123	1507	145	3168	167
348	102	737	124	1559	146	3296	168
360	103	763	125	1613	147	3424	169
372	104	789	126	1669	148	3552	170
385	105	816	127	1727	149	3680	171

3808	172	7776	193	16000	214	32960	235
3936	173	8032	194	16576	215	34112	236
4064	174	8320	195	17152	216	35296	237
4192	175	8608	196	17760	217	36544	238
4352	176	8896	197	18400	218	37824	239
4512	177	9216	198	19040	219	39136	240
4672	178	9536	199	19712	220	40512	241
4832	179	9856	200	20416	221	41920	242
4992	180	10208	201	21120	222	43392	243
5152	181	10560	202	21856	223	44896	244
5344	182	10944	203	22624	224	46464	245
5536	183	11328	204	23424	225	48096	246
5728	184	11744	205	24224	226	49760	247
5920	185	12160	206	25056	227	51488	248
6112	186	12576	207	25920	228	53280	249
6336	187	13024	208	26816	229	55136	250
6560	188	13472	209	27744	230	57056	251
6784	189	13952	210	28704	231	59040	252
7008	190	14432	211	29696	232	61120	253
7264	191	14944	212	30752	233	63264	254
7520	192	15456	213	31840	234	65504	255

APPENDIX D: High Voltage Commanding Tolerance Tables

ELS MCP Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 500 Volts	±60%	2
501-1760 Volts	±30%	2
1760 – 2642 Volts	±10%	2
2643 Volts	No further Commanding	No further Commanding

IBS CEM Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 500 Volts	±40%	16
501-2099	±20%	16
2100 – 2500 Volts	±10%	6
2501 Volts	No further Commanding	No further Commanding

IBS ESA Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 2599 Volts	Disable	Disable
2600 Volts	No further Commanding	No further Commanding

HVU1 ACC Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 2999 Volts	±90%	16
3000 – 6999 Volts	±15%	16
7000 – 11999 Volts	±8 %	16
12000 – 14599 Volts	±5%	8
14600 Volts	No further Commanding	No further Commanding

HVU1 RET Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 2999 Volts	±90%	16
3000 – 6999 Volts	±15%	16
7000 – 11999 Volts	±8 %	16
12000 – 14599 Volts	±5%	8
14600 Volts	No further Commanding	No further Commanding

HVU2 ESA Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 7499 Volts	Disable	Disable
7500 Volts	No further Commanding	No further Commanding

HVU2 LEF Tolerance Table		
Range	**Tolerance**	**Step Size**
1 - 999 Volts	±40%	27
1000 – 2000 Volts	±20%	14
2001 Volts	No further Commanding	No further Commanding

HVU2 ST Tolerance Table		
Range	**Tolerance**	**Step Size**
1 – 999 Volts	±40%	18
1000 – 1999 Volts	±20%	9
2000 – 3000 Volts	±15%	7
3000 Volts	No Further Commanding	No Further Commanding

APPENDIX E: PROM Sequences

Sequence 0 – Actuator Launch Latch Power 1

Time 00:00:00
DPU_HK_FORMAT, MAINT
Time 00:00:00
DPU_HK_MRO, CPU1, CPU1 MEM, 0x20000, 0x20000
Time 00:00:00
ACT_LAT_STATE, ARM
Time 00:00:00
ACT_LAT_CNTRL, ENABLE
Time 00:00:00
DPU_SUPHTR_PWR , OFF
Time 00:01:04
ACT_FOV, IMM, RAM, 0 degree
Time 00:01:04
ACT_EXEC, IMM, 1 dg/s, START
Time 00:01:04
ACT_LATCH, POWER 1 on
Time 00:07:00
ACT_LATCH, POWER 1, off
Time 00:07:00
ACT_FOV, IMM, PARK, 0 degree
Time 00:07:00
DPU_SUPHTR_PWR, ON
Time 00:07:00
ACT_LAT_CNTRL, DISABLE
Time 00:07:00
ACT_LAT_STATE, SAFE
Time 00:07:00
SEQ_END, 0

Sequence 1 – Actuator Launch Latch Power 2

Time 00:00:00
DPU_HK_FORMAT, MAINT
Time 00:00:00
DPU_HK_MRO, CPU1, CPU1 MEM, 0x20000, 0x20000
Time 00:00:00
ACT_LAT_STATE, ARM
Time 00:00:00
ACT_LAT_CNTRL, ENABLE
Time 00:00:00
DPU_SUPHTR_PWR , OFF
Time 00:01:04
ACT_FOV, IMM, RAM, 0 degree
Time 00:01:04
ACT_EXEC, IMM, 1 dg/s, START
Time 00:01:04
ACT_LATCH, POWER 2, on
Time 00:07:00
ACT_LATCH, POWER 2, off
Time 00:07:00
ACT_FOV, IMM, PARK, 0 degree

Time 00:07:00
DPU_SUPHTR_PWR, ON
Time 00:07:00
ACT_LAT_CNTRL, DISABLE
Time 00:07:00
ACT_LAT_STATE, SAFE
Time 00:07:00
SEQ_END, 1

Sequence 2 – IMS Cover Release Power 1

Time 00:00:00
DPU_HK_FORMAT, MAINT
Time 00:00:00
DPU_HK_MRO, CPU1, CPU1 MEM, 0x20000, 0x20000
Time 00:00:00
IMS_COV_STATE, ARM
Time 00:00:00
IMS_COV_CNTRL, ENABLE
Time 00:00:00
DPU_SUPHTR_PWR, OFF
Time 00:01:04
IMS_COVER, Power 1, ON
Time 00:07:00
IMS_COVER, Power 1, OFF
Time 00:07:00
DPU_SUPHTR_PWR, ON
Time 00:07:00
IMS_COV_CNTRL, DISABLE
Time 00:07:00
IMS_COV_STATE, SAFE
Time 00:07:00
SEQ_END, 2

Sequence 3 – IMS Cover Release Power 2

Time 00:00:00
DPU_HK_FORMAT, MAINT
Time 00:00:00
DPU_HK_MRO, CPU1, CPU1 MEM, 0x20000, 0x20000
Time 00:00:00
IMS_COV_STATE, ARM
Time 00:00:00
IMS_COV_CNTRL, ENABLE
Time 00:00:00
DPU_SUPHTR_PWR, OFF
Time 00:01:04
IMS_COVER, Power 2, ON
Time 00:07:00
IMS_COVER, Power 2, OFF

Time 00:07:00
DPU_SUPHTR_PWR, ON
Time 00:07:00
IMS_COV_CNTRL, DISABLE
Time 00:07:00
IMS_COV_STATE, SAFE
Time 00:07:00
SEQ_END, 3

Sequence 4 – Actuator Maintenance

Time 00:00:00
DPU_HK_FORMAT, MAINT
Time 00:00:00
ACT_FOV, IMM, MAINT, 84, 124
Time 00:00:01
ACT_EXEC, IMM, 1, START
Time 00:12:00
ACT_FOV, IMM, MAINT, 84, 124
Time 00:12:00
ACT_EXEC, IMM, 1, START
Time 00:12:00
SEQ_END, 4

APPENDIX F: IBS ESA Sweep and Stim Tables

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
0	48946.42	2576.13	4057			3FDA	2576.51
1	48142.44	2533.81	3991			3F97	2533.97
2	47351.67	2492.19	3925			3F56	2492.70
3	46573.89	2451.26	3861			3F15	2451.43
4	45808.88	2410.99	3797			3ED6	2411.43
5	45056.44	2371.39	3735			3E97	2371.43
6	44316.35	2332.44	3674			3E5A	2332.70
7	43588.43	2294.13	3613			3E1E	2294.60
8	42872.46	2256.45	3554			3DE2	2256.51
9	42168.25	2219.38	3496			3DA8	2219.68
10	41475.60	2182.93	3438			3D6F	2183.49
11	40794.34	2147.07	3382			3D36	2147.30
12	40124.26	2111.80	3326			3CFF	2112.38
13	39465.19	2077.12	3271			3CC8	2077.46
14	38816.95	2043.00	3218			3C92	2043.17
15	38179.36	2009.44	3165			3C5D	2009.52
16	37552.23	1976.43	3113			3C29	1976.51
17	36935.41	1943.97	3062			3BF6	1944.13
18	36328.72	1912.04	3011			3BC4	1912.38
19	35732.00	1880.63	2962			3B92	1880.63
20	35145.08	1849.74	2913			3B62	1850.16
21	34567.79	1819.36	2865			3B32	1819.68
22	33999.99	1789.47	2818			3B03	1789.84
23	33441.52	1760.08	2772			3AD5	1760.63
24	32892.22	1731.17	2727			3AA7	1731.43
25	32351.94	1702.73	2682			3A7A	1702.86
26	31820.54	1674.77	2638			3A4E	1674.92
27	31297.87	1647.26	2594			3A23	1647.62
28	30783.78	1620.20	2552			39F8	1620.32
29	30278.13	1593.59	2510			39CE	1593.65
30	29780.79	1567.41	2469			39A5	1567.62
31	29291.62	1541.66	2428			397D	1542.22
32	28810.49	1516.34	2388			3955	1516.83
33	28337.26	1491.43	2349			392E	1492.06
34	27871.80	1466.94	2310			3907	1467.30
35	27413.98	1442.84	2272			38E1	1443.17
36	26963.69	1419.14	2235			38BC	1419.68
37	26520.79	1395.83	2198			3897	1396.19
38	26085.17	1372.90	2162			3873	1373.33
39	25656.70	1350.35	2127			384F	1350.48
40	25235.27	1328.17	2092			382C	1328.25
41	24820.77	1306.36	2058			380A	1306.67
42	24413.07	1284.90	2024			37E8	1285.08
43	24012.07	1263.79	1990			37C7	1264.13
44	23617.65	1243.03	1958			37A6	1243.17
45	23229.72	1222.62	1926			3786	1222.86
46	22848.15	1202.53	1894			3766	1202.54
47	22472.86	1182.78	1863			3747	1182.86
48	22103.72	1163.35	1832			3729	1163.81
49	21740.65	1144.24	1802			370B	1144.76
50	21383.55	1125.45	1773			36ED	1125.71
51	21032.31	1106.96	1743			36D0	1107.30
52	20686.84	1088.78	1715			36B3	1088.89
53	20347.04	1070.90	1687			3697	1071.11
54	20012.83	1053.31	1659			367B	1053.33
55	19684.10	1036.01	1632			3660	1036.19
56	19360.78	1018.99	1605			3645	1019.05
57	19042.77	1002.25	1579			362B	1002.54
58	18729.97	985.79	1553			3611	986.03
59	18422.32	969.60	1527			35F8	970.16
60	18119.72	953.67	1502			35DF	954.29

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
61	17822.09	938.00	1477			35C6	938.41
62	17529.35	922.60	1453			35AE	923.17
63	17241.42	907.44	1429			3596	907.94
64	16958.22	892.54	1406			357E	892.70
65	16679.67	877.88	1383			3567	878.10
66	16405.69	863.46	1360			3550	863.49
67	16136.22	849.27	1338			353A	849.52
68	15871.17	835.32	1316			3524	835.56
69	15610.48	821.60	1294			350F	822.22
70	15354.06	808.11	1273			34F9	808.25
71	15101.86	794.83	1252			34E4	794.92
72	14853.80	781.78	1231			34D0	782.22
73	14609.82	768.94	1211			34BC	769.52
74	14369.84	756.31	1191			34A8	756.83
75	14133.81	743.88	1172			3494	744.13
76	13901.65	731.67	1152			3481	732.06
77	13673.31	719.65	1133			346E	720.00
78	13448.71	707.83	1115			345B	707.94
79	13227.81	696.20	1097			3449	696.51
80	13010.53	684.76	1079			3437	685.08
81	12796.83	673.52	1061			3425	673.65
82	12586.63	662.45	1043			3414	662.86
83	12379.88	651.57	1026			3403	652.06
84	12176.54	640.87	1009			33F2	641.27
85	11976.53	630.34	993			33E1	630.48
86	11779.81	619.99	976			33D1	620.32
87	11586.31	609.81	960			33C1	610.16
88	11396.00	599.79	945			33B1	600.00
89	11208.81	589.94	929			33A2	590.48
90	11024.70	580.25	914			3392	580.32
91	10843.61	570.72	899			3383	570.79
92	10665.50	561.34	884			3375	561.90
93	10490.31	552.12	870			3366	552.38
94	10318.00	543.05	855			3358	543.49
95	10148.52	534.13	841			334A	534.60
96	9981.82	525.36	827			333C	525.71
97	9817.87	516.73	814			332E	516.83
98	9656.60	508.24	800			3321	508.57
99	9497.98	499.89	787			3314	500.32
100	9341.97	491.68	774			3307	492.06
101	9188.52	483.61	762			32FA	483.81
102	9037.60	475.66	749			32EE	476.19
103	8889.15	467.85	737			32E1	467.94
104	8743.14	460.17	725			32D5	460.32
105	8599.53	452.61	713			32C9	452.70
106	8458.27	445.17	701			32BE	445.71
107	8319.34	437.86	690			32B2	438.10
108	8182.69	430.67	678			32A7	431.11
109	8048.28	423.59	667			329C	424.13
110	7916.08	416.64	656			3291	417.14
111	7786.06	409.79	645			3286	410.16
112	7658.17	403.06	635			327B	403.17
113	7532.37	396.44	624			3271	396.83
114	7408.65	389.93	614			3267	390.48
115	7286.96	383.52	604			325D	384.13
116	7167.26	377.22	594			3253	377.78
117	7049.54	371.03	584			3249	371.43
118	6933.74	364.93	575			323F	365.08
119	6819.85	358.94	565			3236	359.37
120	6707.83	353.04	556			322D	353.65
121	6597.65	347.24	547			3223	347.30
122	6489.28	341.54	538			321A	341.59

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
123	6382.69	335.93	529			3212	336.51
124	6277.85	330.41	520			3209	330.79
125	6174.73	324.99	512			3200	325.08
126	6073.31	319.65	503			31F8	320.00
127	5973.55	314.40	495			31F0	314.92
128	5875.43	309.23	487			31E8	309.84
129	5778.92	304.15	479			31E0	304.76
130	5684.00	299.16	471			31D8	299.68
131	5590.63	294.24	463			31D0	294.60
132	5498.80	289.41	456			31C8	289.52
133	5408.48	284.66	448			31C1	285.08
134	5319.64	279.98	441			31B9	280.00
135	5232.27	275.38	434			31B2	275.56
136	5146.32	270.86	427			31AB	271.11
137	5061.79	266.41	420			31A4	266.67
138	4978.65	262.03	413			319D	262.22
139	4896.87	257.73	406			3196	257.78
140	4816.43	253.50	399			3190	253.97
141	4737.32	249.33	393			3189	249.52
142	4659.51	245.24	386			3183	245.71
143	4582.97	241.21	380			317C	241.27
144	4507.69	237.25	374			3176	237.46
145	4433.65	233.35	368			3170	233.65
146	4360.83	229.52	361			316A	229.84
147	4289.20	225.75	356			3164	226.03
148	4218.74	222.04	350			315E	222.22
149	4149.45	218.39	344			3158	218.41
150	4081.29	214.80	338			3153	215.24
151	4014.25	211.28	333			314D	211.43
152	3948.31	207.81	327			3148	208.25
153	3883.46	204.39	322			3142	204.44
154	3819.67	201.04	317			313D	201.27
155	3756.93	197.73	311			3138	198.10
156	3695.22	194.49	306			3133	194.92
157	3634.53	191.29	301			312E	191.75
158	3574.83	188.15	296			3129	188.57
159	3516.11	185.06	291			3124	185.40
160	3458.35	182.02	287			311F	182.22
161	3401.55	179.03	282			311A	179.05
162	3345.67	176.09	277			3116	176.51
163	3290.72	173.20	273			3111	173.33
164	3236.67	170.35	268			310D	170.79
165	3183.50	167.55	264			3108	167.62
166	3131.21	164.80	260			3104	165.08
167	3079.78	162.09	255			3100	162.54
168	3029.19	159.43	251			30FC	160.00
169	2979.43	156.81	247			30F7	156.83
170	2930.49	154.24	243			30F3	154.29
171	2882.36	151.70	239			30EF	151.75
172	2835.01	149.21	235			30EC	149.84
173	2788.45	146.76	231			30E8	147.30
174	2742.65	144.35	227			30E4	144.76
175	2697.60	141.98	224			30E0	142.22
176	2653.29	139.65	220			30DC	139.68
177	2609.70	137.35	216			30D9	137.78
178	2566.84	135.10	213			30D5	135.24
179	2524.68	132.88	209			30D2	133.33
180	2483.21	130.70	206			30CE	130.79
181	2442.42	128.55	202			30CB	128.89
182	2402.30	126.44	199			30C8	126.98
183	2362.84	124.36	196			30C4	124.44
184	2324.03	122.32	193			30C1	122.54

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
185	2285.85	120.31	189			30BE	120.63
186	2248.31	118.33	186			30BB	118.73
187	2211.38	116.39	183			30B8	116.83
188	2175.05	114.48	180			30B5	114.92
189	2139.33	112.60	177			30B2	113.02
190	2104.19	110.75	174			30AF	111.11
191	2069.62	108.93	172			30AC	109.21
192	2035.63	107.14	169			30A9	107.30
193	2002.19	105.38	166			30A6	105.40
194	1969.31	103.65	163			30A4	104.13
195	1936.96	101.95	161			30A1	102.22
196	1905.14	100.27	158			309E	100.32
197	1873.85	98.62	155			309C	99.05
198	1843.07	97.00	153			3099	97.14
199	1812.80	95.41	150			3097	95.87
200	1783.02	93.84	148			3094	93.97
201	1753.73	92.30	145			3092	92.70
202	1724.93	90.79	143			308F	90.79
203	1696.59	89.29	141			308D	89.52
204	1668.73	87.83	138			308B	88.25
205	1641.32	86.39	136			3089	86.98
206	1614.36	84.97	134			3086	85.08
207	1587.84	83.57	132			3084	83.81
208	1561.76	82.20	129			3082	82.54
209	1536.10	80.85	127			3080	81.27
210	1510.87	79.52	125			307E	80.00
211	1486.06	78.21	123			307C	78.73
212	1461.65	76.93	121			307A	77.46
213	1437.64	75.67	119			3078	76.19
214	1414.02	74.42	117			3076	74.92
215	1390.80	73.20	115			3074	73.65
216	1367.95	72.00	113			3072	72.38
217	1345.48	70.81	112			3070	71.11
218	1323.38	69.65	110			306E	69.84
219	1301.65	68.51		4045		2FCD	-32.38
220	1280.26	67.38		3978		2F8B	-74.29
221	1259.24	66.28		3913		2F49	-116.19
222	1238.55	65.19		3848		2F09	-156.83
223	1218.21	64.12		3785		2ECA	-196.83
224	1198.20	63.06		3723		2E8C	-236.19
225	1178.52	62.03		3662		2E4E	-275.56
226	1159.16	61.01		3602		2E12	61.01
227	1140.12	60.01		3543		2DD7	60.01
228	1121.39	59.02		3484		2D9D	59.03
229	1102.97	58.05		3427		2D64	58.06
230	1084.85	57.10		3371		2D2B	57.10
231	1067.04	56.16		3316		2CF4	56.17
232	1049.51	55.24		3261		2CBE	55.25
233	1032.27	54.33		3208		2C88	54.34
234	1015.31	53.44		3155		2C53	53.44
235	998.64	52.56		3103		2C20	52.58
236	982.23	51.70		3052		2BED	51.71
237	966.10	50.85		3002		2BBA	50.85
238	950.23	50.01		2953		2B89	50.02
239	934.62	49.19		2904		2B59	49.21
240	919.27	48.38		2856		2B29	48.39
241	904.17	47.59		2809		2AFA	47.60
242	889.32	46.81		2763		2ACC	46.82
243	874.71	46.04		2718		2A9E	46.04
244	860.34	45.28		2673		2A72	45.29
245	846.21	44.54		2629		2A46	44.55
246	832.31	43.81		2586		2A1B	43.82

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
247	818.64	43.09		2544		29F0	43.09
248	805.19	42.38		2502		29C6	42.38
249	791.97	41.68		2461		299D	41.69
250	778.96	41.00		2420		2975	41.01
251	766.16	40.32		2381		294D	40.33
252	753.58	39.66		2342		2926	39.67
253	741.20	39.01		2303		2900	39.03
254	729.03	38.37		2265		28DA	38.38
255	717.05	37.74		2228		28B5	37.76
256	705.27	37.12		2191		2890	37.13
257	693.69	36.51		2155		286C	36.52
258	682.30	35.91		2120		2849	35.93
259	671.09	35.32		2085		2826	35.33
260	660.07	34.74		2051		2803	34.74
261	649.22	34.17		2017		27E2	34.18
262	638.56	33.61		1984		27C1	33.62
263	628.07	33.06		1952		27A0	33.06
264	617.75	32.51		1920		2780	32.52
265	607.61	31.98		1888		2760	31.98
266	597.63	31.45		1857		2741	31.45
267	587.81	30.94		1826		2723	30.95
268	578.15	30.43		1796		2705	30.44
269	568.66	29.93		1767		26E7	29.93
270	559.32	29.44		1738		26CA	29.44
271	550.13	28.95		1709		26AE	28.96
272	541.09	28.48		1681		2692	28.49
273	532.21	28.01		1654		2676	28.02
274	523.46	27.55		1627		265B	27.56
275	514.87	27.10		1600		2640	27.10
276	506.41	26.65		1574		2626	26.66
277	498.09	26.22		1548		260C	26.22
278	489.91	25.78		1522		25F3	25.80
279	481.86	25.36		1497		25DA	25.37
280	473.95	24.94		1473		25C1	24.95
281	466.16	24.53		1448		25A9	24.54
282	458.51	24.13		1425		2591	24.14
283	450.97	23.74		1401		257A	23.75
284	443.57	23.35		1378		2563	23.36
285	436.28	22.96		1356		254C	22.97
286	429.11	22.58		1333		2536	22.60
287	422.07	22.21		1311		2520	22.22
288	415.13	21.85		1290		250A	21.85
289	408.31	21.49		1269		24F5	21.49
290	401.61	21.14		1248		24E0	21.14
291	395.01	20.79		1227		24CC	20.80
292	388.52	20.45		1207		24B8	20.46
293	382.14	20.11		1187		24A4	20.12
294	375.86	19.78		1168		2490	19.78
295	369.69	19.46		1149		247D	19.46
296	363.62	19.14		1130		246A	19.14
297	357.65	18.82		1111		2458	18.84
298	351.77	18.51		1093		2446	18.53
299	345.99	18.21		1075		2434	18.23
300	340.31	17.91		1057		2422	17.92
301	334.72	17.62		1040		2411	17.63
302	329.22	17.33		1023		23FF	17.33
303	323.81	17.04		1006		23EF	17.06
304	318.49	16.76		990		23DE	16.77
305	313.26	16.49		973		23CE	16.50
306	308.12	16.22		957		23BE	16.23
307	303.06	15.95		942		23AE	15.96
308	298.08	15.69		926		239F	15.70

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
309	293.18	15.43		911		238F	15.43
310	288.37	15.18		896		2381	15.19
311	283.63	14.93		881		2372	14.94
312	278.97	14.68		867		2363	14.69
313	274.39	14.44		853		2355	14.45
314	269.88	14.20		839		2347	14.21
315	265.45	13.97		825		2339	13.97
316	261.09	13.74		811		232C	13.75
317	256.80	13.52		798		231E	13.52
318	252.58	13.29		785		2311	13.30
319	248.43	13.08		772		2304	13.08
320	244.35	12.86		759		22F8	12.87
321	240.34	12.65		747		22EB	12.65
322	236.39	12.44		735		22DF	12.45
323	232.51	12.24		722		22D3	12.25
324	228.69	12.04		711		22C7	12.04
325	224.93	11.84		699		22BB	11.84
326	221.24	11.64		687		22B0	11.65
327	217.60	11.45		676		22A5	11.47
328	214.03	11.26		665		229A	11.28
329	210.51	11.08		654		228F	11.09
330	207.06	10.90		643		2284	10.91
331	203.66	10.72		633		2279	10.72
332	200.31	10.54		622		226F	10.55
333	197.02	10.37		612		2265	10.38
334	193.78	10.20		602		225B	10.21
335	190.60	10.03		592		2251	10.04
336	187.47	9.87		583		2247	9.88
337	184.39	9.70		573		223D	9.71
338	181.36	9.55		564		2234	9.55
339	178.38	9.39		554		222B	9.40
340	175.45	9.23		545		2222	9.25
341	172.57	9.08		536		2219	9.10
342	169.74	8.93		527		2210	8.94
343	166.95	8.79		519		2207	8.79
344	164.21	8.64		510		21FF	8.66
345	161.51	8.50		502		21F6	8.50
346	158.86	8.36		494		21EE	8.37
347	156.25	8.22		485		21E6	8.23
348	153.68	8.09		478		21DE	8.10
349	151.16	7.96		470		21D6	7.96
350	148.67	7.82		462		21CE	7.83
351	146.23	7.70		454		21C7	7.71
352	143.83	7.57		447		21BF	7.57
353	141.47	7.45		440		21B8	7.45
354	139.14	7.32		432		21B1	7.33
355	136.86	7.20		425		21AA	7.22
356	134.61	7.08		418		21A3	7.10
357	132.40	6.97		411		219C	6.98
358	130.22	6.85		405		2195	6.86
359	128.08	6.74		398		218E	6.74
360	125.98	6.63		391		2188	6.64
361	123.91	6.52		385		2182	6.54
362	121.88	6.41		379		217B	6.42
363	119.87	6.31		372		2175	6.32
364	117.91	6.21		366		216F	6.22
365	115.97	6.10		360		2169	6.11
366	114.06	6.00		354		2163	6.01
367	112.19	5.90		349		215D	5.91
368	110.35	5.81		343		2157	5.81
369	108.53	5.71		337		2152	5.73
370	106.75	5.62		332		214C	5.62

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
371	105.00	5.53		326		2147	5.54
372	103.27	5.44		321		2141	5.44
373	101.58	5.35		316		213C	5.35
374	99.91	5.26		310		2137	5.27
375	98.27	5.17		305		2132	5.18
376	96.65	5.09		300		212D	5.10
377	95.07	5.00		295		2128	5.01
378	93.50	4.92		291		2123	4.93
379	91.97	4.84		286		211E	4.84
380	90.46	4.76		281		211A	4.78
381	88.97	4.68		276		2115	4.69
382	87.51	4.61		272		2110	4.61
383	86.07	4.53		267		210C	4.54
384	84.66	4.46		263		2108	4.47
385	83.27	4.38		259		2103	4.39
386	81.90	4.31		254		20FF	4.32
387	80.56	4.24		250		20FB	4.25
388	79.23	4.17		246		20F7	4.18
389	77.93	4.10		242		20F3	4.12
390	76.65	4.03		238		20EF	4.05
391	75.39	3.97		234		20EB	3.98
392	74.15	3.90		230		20E7	3.91
393	72.94	3.84		227		20E3	3.85
394	71.74	3.78		223		20DF	3.78
395	70.56	3.71		219		20DC	3.73
396	69.40	3.65		216		20D8	3.66
397	68.26	3.59		212		20D5	3.61
398	67.14	3.53		209		20D1	3.54
399	66.04	3.48		205		20CE	3.49
400	64.95	3.42		202		20CA	3.42
401	63.88	3.36		199		20C7	3.37
402	62.84	3.31		195		20C4	3.32
403	61.80	3.25		192		20C1	3.27
404	60.79	3.20		189		20BD	3.20
405	59.79	3.15		186		20BA	3.15
406	58.81	3.10		183		20B7	3.10
407	57.84	3.04		180		20B4	3.05
408	56.89	2.99		177		20B1	3.00
409	55.96	2.95		174		20AE	2.95
410	55.04	2.90		171		20AC	2.91
411	54.13	2.85		168		20A9	2.86
412	53.24	2.80		165		20A6	2.81
413	52.37	2.76		163		20A3	2.76
414	51.51	2.71		160		20A1	2.73
415	50.66	2.67		157		209E	2.68
416	49.83	2.62		155		209B	2.63
417	49.01	2.58		152		2099	2.59
418	48.21	2.54		150		2096	2.54
419	47.42	2.50		147		2094	2.51
420	46.64	2.45		145		2091	2.46
421	45.87	2.41		143		208F	2.42
422	45.12	2.37		140		208D	2.39
423	44.38	2.34		138		208A	2.34
424	43.65	2.30		136		2088	2.30
425	42.93	2.26		133		2086	2.27
426	42.23	2.22		131		2084	2.24
427	41.53	2.19		129		2082	2.20
428	40.85	2.15		127		207F	2.15
429	40.18	2.11		125		207D	2.12
430	39.52	2.08		123		207B	2.08
431	38.87	2.05		121		2079	2.05
432	38.23	2.01		119		2077	2.02

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
433	37.60	1.98		117		2075	1.98
434	36.99	1.95		115		2073	1.95
435	36.38	1.91		113		2072	1.93
436	35.78	1.88		111		2070	1.90
437	35.19	1.85		109		206E	1.86
438	34.61	1.82			4032	1FC0	1.82
439	34.05	1.79			3965	1F7E	1.79
440	33.49	1.76			3900	1F3D	1.76
441	32.94	1.73			3836	1EFD	1.73
442	32.40	1.71			3773	1EBE	1.71
443	31.86	1.68			3711	1E80	1.68
444	31.34	1.65			3650	1E43	1.65
445	30.83	1.62			3590	1E07	1.62
446	30.32	1.60			3531	1DCC	1.60
447	29.82	1.57			3473	1D92	1.57
448	29.33	1.54			3416	1D59	1.54
449	28.85	1.52			3360	1D21	1.52
450	28.38	1.49			3305	1CEA	1.49
451	27.91	1.47			3251	1CB3	1.47
452	27.45	1.44			3197	1C7E	1.45
453	27.00	1.42			3145	1C49	1.42
454	26.56	1.40			3093	1C16	1.40
455	26.12	1.37			3042	1BE3	1.38
456	25.69	1.35			2992	1BB1	1.35
457	25.27	1.33			2943	1B80	1.33
458	24.85	1.31			2895	1B4F	1.31
459	24.45	1.29			2847	1B20	1.29
460	24.04	1.27			2801	1AF1	1.27
461	23.65	1.24			2755	1AC3	1.24
462	23.26	1.22			2709	1A96	1.22
463	22.88	1.20			2665	1A69	1.20
464	22.50	1.18			2621	1A3E	1.18
465	22.13	1.16			2578	1A12	1.16
466	21.77	1.15			2536	19E8	1.15
467	21.41	1.13			2494	19BE	1.13
468	21.06	1.11			2453	1996	1.11
469	20.72	1.09			2413	196D	1.09
470	20.37	1.07			2373	1946	1.07
471	20.04	1.05			2334	191F	1.06
472	19.71	1.04			2296	18F8	1.04
473	19.39	1.02			2258	18D3	1.02
474	19.07	1.00			2221	18AD	1.00
475	18.76	0.99			2185	1889	0.99
476	18.45	0.97			2149	1865	0.97
477	18.14	0.95			2113	1842	0.96
478	17.85	0.94			2079	181F	0.94
479	17.55	0.92			2044	17FD	0.92
480	17.26	0.91			2011	17DB	0.91
481	16.98	0.89			1978	17BA	0.89
482	16.70	0.88			1945	179A	0.88
483	16.43	0.86			1913	177A	0.86
484	16.16	0.85			1882	175A	0.85
485	15.89	0.84			1851	173C	0.84
486	15.63	0.82			1821	171D	0.82
487	15.38	0.81			1791	16FF	0.81
488	15.12	0.80			1761	16E2	0.80
489	14.87	0.78			1732	16C5	0.78
490	14.63	0.77			1704	16A8	0.77
491	14.39	0.76			1676	168C	0.76
492	14.15	0.74			1648	1671	0.75
493	13.92	0.73			1621	1656	0.73
494	13.69	0.72			1595	163B	0.72

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
495	13.47	0.71			1569	1621	0.71
496	13.25	0.70			1543	1607	0.70
497	13.03	0.69			1517	15EE	0.69
498	12.81	0.67			1493	15D5	0.67
499	12.60	0.66			1468	15BC	0.66
500	12.40	0.65			1444	15A4	0.65
501	12.19	0.64			1420	158D	0.64
502	11.99	0.63			1397	1575	0.63
503	11.80	0.62			1374	155E	0.62
504	11.60	0.61			1351	1548	0.61
505	11.41	0.60			1329	1532	0.60
506	11.22	0.59			1307	151C	0.59
507	11.04	0.58			1286	1506	0.58
508	10.86	0.57			1265	14F1	0.57
509	10.68	0.56			1244	14DC	0.56
510	10.50	0.55			1224	14C8	0.55
511	10.33	0.54			1203	14B4	0.54
512	10.16	0.53			1184	14A0	0.54
513	10.00	0.53			1164	148D	0.53
514	9.83	0.52			1145	147A	0.52
515	9.67	0.51			1126	1467	0.51
516	9.51	0.50			1108	1454	0.50
517	9.35	0.49			1090	1442	0.49
518	9.20	0.48			1072	1430	0.48
519	9.05	0.48			1054	141F	0.48
520	8.90	0.47			1037	140D	0.47
521	8.76	0.46			1020	13FC	0.46
522	8.61	0.45			1003	13EB	0.45
523	8.47	0.45			987	13DB	0.45
524	8.33	0.44			970	13CB	0.44
525	8.19	0.43			954	13BB	0.43
526	8.06	0.42			939	13AB	0.42
527	7.93	0.42			923	139C	0.42
528	7.80	0.41			908	138D	0.41
529	7.67	0.40			893	137E	0.40
530	7.54	0.40			879	136F	0.40
531	7.42	0.39			864	1361	0.39
532	7.30	0.38			850	1352	0.38
533	7.18	0.38			836	1344	0.38
534	7.06	0.37			822	1337	0.37
535	6.94	0.37			809	1329	0.37
536	6.83	0.36			795	131C	0.36
537	6.72	0.35			782	130F	0.35
538	6.61	0.35			769	1302	0.35
539	6.50	0.34			757	12F5	0.34
540	6.39	0.34			744	12E9	0.34
541	6.29	0.33			732	12DD	0.33
542	6.18	0.33			720	12D1	0.33
543	6.08	0.32			708	12C5	0.32
544	5.98	0.31			697	12B9	0.31
545	5.88	0.31			685	12AE	0.31
546	5.79	0.30			674	12A3	0.31
547	5.69	0.30			663	1297	0.30
548	5.60	0.29			652	128D	0.30
549	5.51	0.29			641	1282	0.29
550	5.42	0.29			631	1277	0.29
551	5.33	0.28			620	126D	0.28
552	5.24	0.28			610	1263	0.28
553	5.15	0.27			600	1259	0.27
554	5.07	0.27			590	124F	0.27
555	4.99	0.26			581	1245	0.26
556	4.90	0.26			571	123C	0.26

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
557	4.82	0.25			562	1232	0.25
558	4.74	0.25			553	1229	0.25
559	4.67	0.25			543	1220	0.25
560	4.59	0.24			535	1217	0.24
561	4.51	0.24			526	120E	0.24
562	4.44	0.23			517	1206	0.23
563	4.37	0.23			509	11FD	0.23
564	4.30	0.23			500	11F5	0.23
565	4.22	0.22			492	11ED	0.22
566	4.16	0.22			484	11E4	0.22
567	4.09	0.22			476	11DD	0.22
568	4.02	0.21			468	11D5	0.21
569	3.95	0.21			460	11CD	0.21
570	3.89	0.20			453	11C5	0.20
571	3.82	0.20			445	11BE	0.20
572	3.76	0.20			438	11B7	0.20
573	3.70	0.19			431	11AF	0.19
574	3.64	0.19			424	11A8	0.19
575	3.58	0.19			417	11A1	0.19
576	3.52	0.19			410	119B	0.19
577	3.46	0.18			403	1194	0.18
578	3.41	0.18			397	118D	0.18
579	3.35	0.18			390	1187	0.18
580	3.30	0.17			384	1180	0.17
581	3.24	0.17			377	117A	0.17
582	3.19	0.17			371	1174	0.17
583	3.14	0.17			365	116E	0.17
584	3.08	0.16			359	1168	0.16
585	3.03	0.16			353	1162	0.16
586	2.98	0.16			347	115C	0.16
587	2.93	0.15			342	1156	0.15
588	2.89	0.15			336	1151	0.15
589	2.84	0.15			331	114B	0.15
590	2.79	0.15			325	1146	0.15
591	2.75	0.14			320	1140	0.14
592	2.70	0.14			315	113B	0.14
593	2.66	0.14			309	1136	0.14
594	2.61	0.14			304	1131	0.14
595	2.57	0.14			299	112C	0.14
596	2.53	0.13			294	1127	0.13
597	2.49	0.13			290	1122	0.13
598	2.45	0.13			285	111D	0.13
599	2.41	0.13			280	1119	0.13
600	2.37	0.12			276	1114	0.12
601	2.33	0.12			271	1110	0.12
602	2.29	0.12			267	110B	0.12
603	2.25	0.12			262	1107	0.12
604	2.21	0.12			258	1102	0.12
605	2.18	0.11			254	10FE	0.11
606	2.14	0.11			250	10FA	0.11
607	2.11	0.11			245	10F6	0.11
608	2.07	0.11			241	10F2	0.11
609	2.04	0.11			237	10EE	0.11
610	2.00	0.11			234	10EA	0.11
611	1.97	0.10			230	10E6	0.10
612	1.94	0.10			226	10E2	0.10
613	1.91	0.10			222	10DF	0.10
614	1.88	0.10			219	10DB	0.10
615	1.85	0.10			215	10D7	0.10
616	1.82	0.10			211	10D4	0.10
617	1.79	0.09			208	10D0	0.09
618	1.76	0.09			205	10CD	0.09

Index	Energy (eV)	ESA (V)	DAC Hi	DAC Mid	DAC Low	Cmd Value	Actual ESA (V)
619	1.73	0.09			201	10CA	0.09
620	1.70	0.09			198	10C6	0.09
621	1.67	0.09			195	10C3	0.09
622	1.64	0.09			191	10C0	0.09
623	1.62	0.09			188	10BD	0.09
624	1.59	0.08			185	10BA	0.08
625	1.56	0.08			182	10B7	0.08
626	1.54	0.08			179	10B4	0.08
627	1.51	0.08			176	10B1	0.08
628	1.49	0.08			173	10AE	0.08
629	1.46	0.08			170	10AB	0.08
630	1.44	0.08			168	10A8	0.08
631	1.42	0.07			165	10A5	0.07
632	1.39	0.07			162	10A3	0.07
633	1.37	0.07			160	10A0	0.07
634	1.35	0.07			157	109D	0.07
635	1.33	0.07			154	109B	0.07
636	1.30	0.07			152	1098	0.07
637	1.28	0.07			149	1096	0.07
638	1.26	0.07			147	1093	0.07
639	1.24	0.07			144	1091	0.07
640	1.22	0.06			142	108F	0.06
641	1.20	0.06			140	108C	0.06
642	1.18	0.06			137	108A	0.06
643	1.16	0.06			135	1088	0.06
644	1.14	0.06			133	1085	0.06
645	1.12	0.06			131	1083	0.06
646	1.10	0.06			129	1081	0.06
647	1.09	0.06			127	107F	0.06
648	1.07	0.06			124	107D	0.06
649	1.05	0.06			122	107B	0.06
650	1.03	0.05			120	1079	0.05
651	1.02	0.05			118	1077	0.05
652	1.00	0.05			116	1075	0.05

Table 1 Solar Wind Search Table

Step	Index	Step	Index	Step	Index	Step	Index
0	96	64	160	128	224	192	288
1	97	65	161	129	225	193	289
2	98	66	162	130	226	194	290
3	99	67	163	131	227	195	291
4	100	68	164	132	228	196	292
5	101	69	165	133	229	197	293
6	102	70	166	134	230	198	294
7	103	71	167	135	231	199	295
8	104	72	168	136	232	200	296
9	105	73	169	137	233	201	297
10	106	74	170	138	234	202	298
11	107	75	171	139	235	203	299
12	108	76	172	140	236	204	300
13	109	77	173	141	237	205	301
14	110	78	174	142	238	206	302
15	111	79	175	143	239	207	303
16	112	80	176	144	240	208	304
17	113	81	177	145	241	209	305
18	114	82	178	146	242	210	306
19	115	83	179	147	243	211	307
20	116	84	180	148	244	212	308
21	117	85	181	149	245	213	309
22	118	86	182	150	246	214	310
23	119	87	183	151	247	215	311
24	120	88	184	152	248	216	312
25	121	89	185	153	249	217	313
26	122	90	186	154	250	218	314
27	123	91	187	155	251	219	315
28	124	92	188	156	252	220	316
29	125	93	189	157	253	221	317
30	126	94	190	158	254	222	318
31	127	95	191	159	255	223	319
32	128	96	192	160	256	224	320
33	129	97	193	161	257	225	321
34	130	98	194	162	258	226	322
35	131	99	195	163	259	227	323
36	132	100	196	164	260	228	324
37	133	101	197	165	261	229	325
38	134	102	198	166	262	230	326
39	135	103	199	167	263	231	327
40	136	104	200	168	264	232	328
41	137	105	201	169	265	233	329
42	138	106	202	170	266	234	330
43	139	107	203	171	267	235	331
44	140	108	204	172	268	236	332
45	141	109	205	173	269	237	333
46	142	110	206	174	270	238	334
47	143	111	207	175	271	239	335
48	144	112	208	176	272	240	336
49	145	113	209	177	273	241	337
50	146	114	210	178	274	242	338
51	147	115	211	179	275	243	339
52	148	116	212	180	276	244	340
53	149	117	213	181	277	245	341
54	150	118	214	182	278	246	342
55	151	119	215	183	279	247	343
56	152	120	216	184	280	248	344
57	153	121	217	185	281	249	345
58	154	122	218	186	282	250	346
59	155	123	219	187	283	251	347
60	156	124	220	188	284	252	348
61	157	125	221	189	285	253	349

62	158	126	222	190	286	254	95
63	159	127	223	191	287	255	95

Table 2 Mag. Mode Sweep 1

Step	Index	Step	Index	Step	Index	Step	Index
0	7	64	135	128	263	192	391
1	9	65	137	129	265	193	393
2	11	66	139	130	267	194	395
3	13	67	141	131	269	195	397
4	15	68	143	132	271	196	399
5	17	69	145	133	273	197	401
6	19	70	147	134	275	198	403
7	21	71	149	135	277	199	405
8	23	72	151	136	279	200	407
9	25	73	153	137	281	201	409
10	27	74	155	138	283	202	411
11	29	75	157	139	285	203	413
12	31	76	159	140	287	204	415
13	33	77	161	141	289	205	417
14	35	78	163	142	291	206	419
15	37	79	165	143	293	207	421
16	39	80	167	144	295	208	423
17	41	81	169	145	297	209	425
18	43	82	171	146	299	210	427
19	45	83	173	147	301	211	429
20	47	84	175	148	303	212	431
21	49	85	177	149	305	213	433
22	51	86	179	150	307	214	435
23	53	87	181	151	309	215	437
24	55	88	183	152	311	216	439
25	57	89	185	153	313	217	441
26	59	90	187	154	315	218	443
27	61	91	189	155	317	219	445
28	63	92	191	156	319	220	447
29	65	93	193	157	321	221	449
30	67	94	195	158	323	222	451
31	69	95	197	159	325	223	453
32	71	96	199	160	327	224	455
33	73	97	201	161	329	225	457
34	75	98	203	162	331	226	459
35	77	99	205	163	333	227	461
36	79	100	207	164	335	228	463
37	81	101	209	165	337	229	465
38	83	102	211	166	339	230	467
39	85	103	213	167	341	231	469
40	87	104	215	168	343	232	471
41	89	105	217	169	345	233	473
42	91	106	219	170	347	234	475
43	93	107	221	171	349	235	477
44	95	108	223	172	351	236	479
45	97	109	225	173	353	237	481
46	99	110	227	174	355	238	483
47	101	111	229	175	357	239	485
48	103	112	231	176	359	240	487
49	105	113	233	177	361	241	489
50	107	114	235	178	363	242	491
51	109	115	237	179	365	243	493
52	111	116	239	180	367	244	495
53	113	117	241	181	369	245	497
54	115	118	243	182	371	246	499
55	117	119	245	183	373	247	501
56	119	120	247	184	375	248	503
57	121	121	249	185	377	249	505
58	123	122	251	186	379	250	507

59	125	123	253	187	381	251	509
60	127	124	255	188	383	252	511
61	129	125	257	189	385	253	513
62	131	126	259	190	387	254	5
63	133	127	261	191	389	255	5

Table 3 Mag. Mode Sweep 2

Step	Index	Step	Index	Step	Index	Step	Index
0	6	64	134	128	262	192	390
1	8	65	136	129	264	193	392
2	10	66	138	130	266	194	394
3	12	67	140	131	268	195	396
4	14	68	142	132	270	196	398
5	16	69	144	133	272	197	400
6	18	70	146	134	274	198	402
7	20	71	148	135	276	199	404
8	22	72	150	136	278	200	406
9	24	73	152	137	280	201	408
10	26	74	154	138	282	202	410
11	28	75	156	139	284	203	412
12	30	76	158	140	286	204	414
13	32	77	160	141	288	205	416
14	34	78	162	142	290	206	418
15	36	79	164	143	292	207	420
16	38	80	166	144	294	208	422
17	40	81	168	145	296	209	424
18	42	82	170	146	298	210	426
19	44	83	172	147	300	211	428
20	46	84	174	148	302	212	430
21	48	85	176	149	304	213	432
22	50	86	178	150	306	214	434
23	52	87	180	151	308	215	436
24	54	88	182	152	310	216	438
25	56	89	184	153	312	217	440
26	58	90	186	154	314	218	442
27	60	91	188	155	316	219	444
28	62	92	190	156	318	220	446
29	64	93	192	157	320	221	448
30	66	94	194	158	322	222	450
31	68	95	196	159	324	223	452
32	70	96	198	160	326	224	454
33	72	97	200	161	328	225	456
34	74	98	202	162	330	226	458
35	76	99	204	163	332	227	460
36	78	100	206	164	334	228	462
37	80	101	208	165	336	229	464
38	82	102	210	166	338	230	466
39	84	103	212	167	340	231	468
40	86	104	214	168	342	232	470
41	88	105	216	169	344	233	472
42	90	106	218	170	346	234	474
43	92	107	220	171	348	235	476
44	94	108	222	172	350	236	478
45	96	109	224	173	352	237	480
46	98	110	226	174	354	238	482
47	100	111	228	175	356	239	484
48	102	112	230	176	358	240	486
49	104	113	232	177	360	241	488
50	106	114	234	178	362	242	490
51	108	115	236	179	364	243	492
52	110	116	238	180	366	244	494
53	112	117	240	181	368	245	496
54	114	118	242	182	370	246	498
55	116	119	244	183	372	247	500
56	118	120	246	184	374	248	502
57	120	121	248	185	376	249	504
58	122	122	250	186	378	250	506
59	124	123	252	187	380	251	508
60	126	124	254	188	382	252	510
61	128	125	256	189	384	253	512

62	130	126	258	190	386	254	4
63	132	127	260	191	388	255	4

IBS Stim Table 1					
Step	**Stim Value**	**Step**	**Stim Value**	**Step**	**Stim Value**
0	0	48	5	96	11
1	0	49	5	97	11
2	1	50	4	98	10
3	1	51	4	99	10
4	2	52	3	100	9
5	2	53	3	101	9
6	3	54	2	102	8
7	3	55	2	103	8
8	4	56	1	104	7
9	4	57	1	105	7
10	5	58	0	106	6
11	5	59	0	107	6
12	6	60	0	108	5
13	6	61	0	109	5
14	7	62	1	110	4
15	7	63	1	111	4
16	8	64	2	112	3
17	8	65	2	113	3
18	9	66	3	114	2
19	9	67	3	115	2
20	10	68	4	116	1
21	10	69	4	117	1
22	11	70	5	118	0
23	11	71	5	119	0
24	12	72	6	120	0
25	12	73	6	121	0
26	13	74	7	122	0
27	13	75	7	123	0
28	14	76	8	124	0
29	14	77	8	125	0
30	14	78	9	126	0
31	14	79	9	127	0
32	13	80	10	128	0
33	13	81	10	129	0
34	12	82	11	130	1
35	12	83	11	131	1
36	11	84	12	132	2
37	11	85	12	133	2
38	10	86	13	134	3
39	10	87	13	135	3
40	9	88	14	136	4
41	9	89	14	137	4
42	8	90	14	138	5
43	8	91	14	139	5
44	7	92	13	140	6
45	7	93	13	141	6
46	6	94	12	142	7
47	6	95	12	143	7
144	8	193	2	242	2

IBS Stim Table 1					
Step	**Stim Value**	**Step**	**Stim Value**	**Step**	**Stim Value**
145	8	194	3	243	2
146	9	195	3	244	1
147	9	196	4	245	1
148	10	197	4	246	0
149	10	198	5	247	0
150	11	199	5	248	0
151	11	200	6	249	0
152	12	201	6	250	0
153	12	202	7	251	0
154	13	203	7	252	0
155	13	204	8	253	0
156	14	205	8	254	0
157	14	206	9	255	0
158	14	207	9		
159	14	208	10		
160	13	209	10		
161	13	210	11		
162	12	211	11		
163	12	212	12		
164	11	213	12		
165	11	214	13		
166	10	215	13		
167	10	216	14		
168	9	217	14		
169	9	218	14		
170	8	219	14		
171	8	220	13		
172	7	221	13		
173	7	222	12		
174	6	223	12		
175	6	224	11		
176	5	225	11		
177	5	226	10		
178	4	227	10		
179	4	228	9		
180	3	229	9		
181	3	230	8		
182	2	231	8		
183	2	232	7		
184	1	233	7		
185	1	234	6		
186	0	235	6		
187	0	236	5		
188	0	237	5		
189	0	238	4		
190	1	239	4		
191	1	240	3		
192	2	241	3		

IBS Stim Table 2					
Step	**Stim Value**	**Step**	**Stim Value**	**Step**	**Stim Value**
0	0	48	4	96	10
1	0	49	4	97	10
2	0	50	4	98	10
3	0	51	4	99	10
4	2	52	2	100	8
5	2	53	2	101	8
6	2	54	2	102	8
7	2	55	2	103	8
8	4	56	0	104	6
9	4	57	0	105	6
10	4	58	0	106	6
11	4	59	0	107	6
12	6	60	0	108	4
13	6	61	0	109	4
14	6	62	0	110	4
15	6	63	0	111	4
16	8	64	2	112	2
17	8	65	2	113	2
18	8	66	2	114	2
19	8	67	2	115	2
20	10	68	4	116	0
21	10	69	4	117	0
22	10	70	4	118	0
23	10	71	4	119	0
24	12	72	6	120	0
25	12	73	6	121	0
26	12	74	6	122	0
27	12	75	6	123	0
28	14	76	8	124	0
29	14	77	8	125	0
30	14	78	8	126	0
31	14	79	8	127	0
32	12	80	10	128	0
33	12	81	10	129	0
34	12	82	10	130	0
35	12	83	10	131	0
36	10	84	12	132	2
37	10	85	12	133	2
38	10	86	12	134	2
39	10	87	12	135	2
40	8	88	14	136	4
41	8	89	14	137	4
42	8	90	14	138	4
43	8	91	14	139	4
44	6	92	12	140	6
45	6	93	12	141	6
46	6	94	12	142	6
47	6	95	12	143	6
144	8	193	2	242	2

IBS Stim Table 2					
Step	**Stim Value**	**Step**	**Stim Value**	**Step**	**Stim Value**
145	8	194	2	243	2
146	8	195	2	244	0
147	8	196	4	245	0
148	10	197	4	246	0
149	10	198	4	247	0
150	10	199	4	248	0
151	10	200	6	249	0
152	12	201	6	250	0
153	12	202	6	251	0
154	12	203	6	252	0
155	12	204	8	253	0
156	14	205	8	254	0
157	14	206	8	255	0
158	14	207	8		
159	14	208	10		
160	12	209	10		
161	12	210	10		
162	12	211	10		
163	12	212	12		
164	10	213	12		
165	10	214	12		
166	10	215	12		
167	10	216	14		
168	8	217	14		
169	8	218	14		
170	8	219	14		
171	8	220	12		
172	6	221	12		
173	6	222	12		
174	6	223	12		
175	6	224	10		
176	4	225	10		
177	4	226	10		
178	4	227	10		
179	4	228	8		
180	2	229	8		
181	2	230	8		
182	2	231	8		
183	2	232	6		
184	0	233	6		
185	0	234	6		
186	0	235	6		
187	0	236	4		
188	0	237	4		
189	0	238	4		
190	0	239	4		
191	0	240	2		
192	2	241	2		

APPENDIX G: HVU2 ESA Sweep Tables

Default HVU2 ESA Sweep Table					
Step	**Voltage**	**DAC Value (hex)**	**Step**	**Voltage**	**DAC Value (hex)**
0	7415.0008	3FFF	45	3.0446	1983
1	6234.3950	3D73	46	2.5594	17FF
2	5243.3950	3B50	47	2.1531	16BA
3	4409.1641	3983	48	1.8105	15A8
4	3706.5950	37FF	49	1.5217	14C1
5	3118.1029	36BA	50	1.2803	1400
6	2621.9588	35A8	51	1.0765	135D
7	2203.6767	34C1	52	0.9052	12D4
8	1854.2029	3400	53	0.7615	1261
9	1559.0514	335D	54	0.6402	1299
10	1310.9794	32D4	55	0.5376	11AE
11	1102.7437	3261	56	0.4526	116A
12	927.1014	3200	57	0.3801	1130
13	778.6204	31AE	58	0.3201	1100
14	655.4897	316A	59	0.2688	10D7
15	550.4665	3130	60	0.2263	10B5
16	463.5507	3100	61	0.1901	1098
17	389.3102	30D7	62	0.1600	1080
18	327.7448	30B5	63	7415.0008	3FFF
19	275.2332	3098			
20	231.7754	3080			
21	194.8471	2FFF			
22	163.8238	2D73			
23	137.7966	2B50			
24	115.8614	2983			
25	97.3997	27FF			
26	81.9357	26BA			
27	68.8983	25A8			
28	57.9069	24C1			
29	48.7237	2400			
30	40.9678	235D			
31	34.4492	22D4			
32	28.9773	2261			
33	24.3618	2200			
34	20.4601	21AE			
35	17.2246	216A			
36	14.4648	2130			
37	12.1809	2100			
38	10.2301	20D7			
39	8.6123	20B5			
40	7.2324	2098			
41	6.0905	2080			
42	5.1201	1FFF			
43	4.3049	1D73			
44	3.6210	1B50			

APPENDIX H: BIU Descriptor Table Configuration

BIU Subaddress Descriptor Table 1								
Subaddress	**Control Word**					**Status List Pointer**	**Data List Pointer**	**Unused**
	Illegal BroadCast	**Illegal Subaddress**	**Interrupt Upon Valid Command**	**Interrupt When Index = 0**	**Index**			
Receive 1	No	No	No	No	0	C4FF	0404	C4FF
Receive 2	No	No	No	No	0	0181	0400	0181
Receive 3	No	No	No	No	0	0182	E000	E182
Receive 4	Yes	Yes	No	No	0	0183	01E0	01E3
Receive 5	Yes	Yes	No	No	0	0184	01E0	01E4
Receive 6	Yes	Yes	No	No	0	0185	01E0	01E5
Receive 7	No	No	No	No	3F	0800	128C	0000
Receive 8	No	No	No	No	3F	083F	168C	0000
Receive 9	No	No	No	No	3F	087E	178C	0000
Receive 10	No	No	No	No	2	08BD	188C	01E9
Receive 11	Yes	Yes	No	No	0	018A	01E0	01EA
Receive 12	Yes	Yes	No	No	0	018B	01E0	01EB
Receive 13	Yes	Yes	No	No	0	018C	01E0	01EC
Receive 14	No	No	No	No	0	018D	01E0	01ED
Receive 15	Yes	Yes	No	No	0	018E	01E0	01EE
Receive 16	Yes	Yes	No	No	0	018F	01E0	01EF
Receive 17	Yes	Yes	No	No	0	0190	01E0	01F0
Receive 18	No	No	No	No	0	0191	01E0	01F1
Receive 19	No	No	No	No	0	0192	01E0	01F2
Receive 20	Yes	Yes	No	No	0	0193	01E0	01F3
Receive 21	Yes	Yes	No	No	0	0194	01E0	01F4
Receive 22	Yes	Yes	No	No	0	0195	01E0	01F5
Receive 23	Yes	Yes	No	No	0	0196	01E0	01F6
Receive 24	Yes	Yes	No	No	0	0197	01E0	01F7
Receive 25	Yes	Yes	No	No	0	0198	01E0	01F8
Receive 26	Yes	Yes	No	No	0	0199	01E0	01F9
Receive 27	Yes	Yes	No	No	0	019A	01E0	01FA
Receive 28	Yes	Yes	No	No	0	019B	01E0	01FB
Receive 29	No	No	No	No	1	08BF	18CC	0000
Receive 30	No	No	No	No	0	019D	0160	01FD
Receive 31	No	No	No	No	0	019E	01E0	01FE
Unused	No	No	No	No	0	019F	01E0	01FF
Transmit 1	No	No	No	No	0	C4FF	0404	C4FF
Transmit 2	No	No	No	No	0	01A1	0400	01A1

BIU Subaddress Descriptor Table 1								
Subaddress	**Control Word**					**Status List Pointer**	**Data List Pointer**	**Unused**
	Illegal BroadCast	**Illegal Subaddress**	**Interrupt Upon Valid Command**	**Interrupt When Index = 0**	**Index**			
Transmit 3	No	No	No	No	0	01A2	E000	E1A2
Transmit 4	No	Yes	No	No	0	01A3	0000	01A3
Transmit 5	No	Yes	No	No	0	01A4	0000	01A4
Transmit 6	No	Yes	No	No	0	01A5	0000	01A5
Transmit 7	No	No	No	No	3F	0800	128C	0000
Transmit 8	No	No	No	No	3F	083F	168C	0000
Transmit 9	No	No	No	No	3F	087E	178C	0000
Transmit 10	No	No	No	No	0	08BD	188C	01A9
Transmit 11	No	No	No	No	0	0982	09CA	0000
Transmit 12	No	No	No	No	0	09A2	0DCA	0000
Transmit 13	No	No	No	No	0	01AC	0000	01AC
Transmit 14	No	Yes	No	No	0	01AD	0000	01AD
Transmit 15	No	Yes	No	No	0	01AE	0000	01AE
Transmit 16	No	Yes	No	No	0	01AF	0000	01AF
Transmit 17	No	Yes	No	No	0	01B0	0000	01B0
Transmit 18	No	Yes	No	No	0	01B1	0000	01B1
Transmit 19	No	Yes	No	No	0	01B2	0000	01B2
Transmit 20	No	Yes	No	No	0	01B3	0000	01B3
Transmit 21	No	Yes	No	No	0	01B4	0000	01B4
Transmit 22	No	Yes	No	No	0	01B5	0000	01B5
Transmit 23	No	Yes	No	No	0	01B6	0000	01B6
Transmit 24	No	Yes	No	No	0	01B7	0000	01B7
Transmit 25	No	Yes	No	No	0	01B8	0000	01B8
Transmit 26	No	Yes	No	No	0	01B9	0000	01B9
Transmit 27	No	Yes	No	No	0	01BA	0000	01BA
Transmit 28	No	Yes	No	No	0	01BB	0000	01BB
Transmit 29	No	No	No	No	1	08BF	18CC	0000
Transmit 30	No	No	No	No	0	01BD	0160	01FD
Transmit 31	No	No	No	No	0	01BE	0000	01BE
Unused	No	No	No	No	0	01BF	0000	01BF

BIU Subaddress Descriptor Table 2								
Subaddress	Control Word					Status List Pointer	Data List Pointer	Unused
	Illegal BroadCast	Illegal Subaddress	Interrupt Upon Valid Command	Interrupt When Index = 0	Index			
Receive 1	No	No	No	No	0	C4FF	0604	C4FF
Receive 2	No	No	No	No	0	0181	0600	0181
Receive 3	No	No	No	No	0	0182	E000	E182
Receive 4	Yes	Yes	No	No	0	0183	01E0	01E3
Receive 5	Yes	Yes	No	No	0	0184	01E0	01E4
Receive 6	Yes	Yes	No	No	0	0185	01E0	01E5
Receive 7	No	No	No	No	3F	08C1	18D5	0000
Receive 8	No	No	No	No	3F	0900	1CD5	0000
Receive 9	No	No	No	No	3F	093F	1DD5	0000
Receive 10	No	No	No	No	2	097E	1ED5	01E9
Receive 11	Yes	Yes	No	No	0	018A	01E0	01EA
Receive 12	Yes	Yes	No	No	0	018B	01E0	01EB
Receive 13	Yes	Yes	No	No	0	018C	01E0	01EC
Receive 14	No	No	No	No	0	018D	01E0	01ED
Receive 15	Yes	Yes	No	No	0	018E	01E0	01EE
Receive 16	Yes	Yes	No	No	0	018F	01E0	01EF
Receive 17	Yes	Yes	No	No	0	0190	01E0	01F0
Receive 18	No	No	No	No	0	0191	01E0	01F1
Receive 19	No	No	No	No	0	0192	01E0	01F2
Receive 20	Yes	Yes	No	No	0	0193	01E0	01F3
Receive 21	Yes	Yes	No	No	0	0194	01E0	01F4
Receive 22	Yes	Yes	No	No	0	0195	01E0	01F5
Receive 23	Yes	Yes	No	No	0	0196	01E0	01F6
Receive 24	Yes	Yes	No	No	0	0197	01E0	01F7
Receive 25	Yes	Yes	No	No	0	0198	01E0	01F8
Receive 26	Yes	Yes	No	No	0	0199	01E0	01F9
Receive 27	Yes	Yes	No	No	0	019A	01E0	01FA
Receive 28	Yes	Yes	No	No	0	019B	01E0	01FB
Receive 29	No	No	No	No	1	0980	1F15	0000
Receive 30	No	No	No	No	0	019D	0160	01FD
Receive 31	No	No	No	No	0	019E	01E0	01FE
Unused	No	No	No	No	0	019F	01E0	01FF

BIU Subaddress Descriptor Table 2								
Subaddress	Control Word					Status List Pointer	Data List Pointer	Unused
	Illegal BroadCast	Illegal Subaddress	Interrupt Upon Valid Command	Interrupt When Index = 0	Index			
Transmit 1	No	No	No	No	0	C4FF	0604	C4FF
Transmit 2	No	No	No	No	0	01A1	0600	01A1
Transmit 3	No	No	No	No	0	01A2	E000	E1A2
Transmit 4	No	Yes	No	No	0	01A3	0000	01A3
Transmit 5	No	Yes	No	No	0	01A4	0000	01A4
Transmit 6	No	Yes	No	No	0	01A5	0000	01A5
Transmit 7	No	No	No	No	3F	08C1	18D5	0000
Transmit 8	No	No	No	No	3F	0900	1CD5	0000
Transmit 9	No	No	No	No	3F	093F	1DD5	0000
Transmit 10	No	No	No	No	0	097E	1ED5	01A9
Transmit 11	No	No	No	No	0	09A6	0E2B	0000
Transmit 12	No	No	No	No	0	09C6	122B	0000
Transmit 13	No	No	No	No	0	01AC	0000	01AC
Transmit 14	No	Yes	No	No	0	01AD	0000	01AD
Transmit 15	No	Yes	No	No	0	01AE	0000	01AE
Transmit 16	No	Yes	No	No	0	01AF	0000	01AF
Transmit 17	No	Yes	No	No	0	01B0	0000	01B0
Transmit 18	No	Yes	No	No	0	01B1	0000	01B1
Transmit 19	No	Yes	No	No	0	01B2	0000	01B2
Transmit 20	No	Yes	No	No	0	01B3	0000	01B3
Transmit 21	No	Yes	No	No	0	01B4	0000	01B4
Transmit 22	No	Yes	No	No	0	01B5	0000	01B5
Transmit 23	No	Yes	No	No	0	01B6	0000	01B6
Transmit 24	No	Yes	No	No	0	01B7	0000	01B7
Transmit 25	No	Yes	No	No	0	01B8	0000	01B8
Transmit 26	No	Yes	No	No	0	01B9	0000	01B9
Transmit 27	No	Yes	No	No	0	01BA	0000	01BA
Transmit 28	No	Yes	No	No	0	01BB	0000	01BB
Transmit 29	No	No	No	No	1	0980	1F15	0000
Transmit 30	No	No	No	No	0	01BD	0160	01FD
Transmit 31	No	No	No	No	0	01BE	0000	01BE
Unused	No	No	No	No	0	01BF	0000	01BF

BIU Mode Code Descriptor Table 1												
Mode Code	Control Word									Status List Pointer	Data List Pointer	Unused
	Interrupt On Receipt (w/o)	Illegalize Broadcast (w/o)	Illegalize Mode Code (w/o)	Reserved	Illegalize Broadcast (with data)	Illegalize Transmit (with data)	Illegalize Receive (with data)	Interrupt On Receipt	Index			
0 & 16	No	No	Yes	0	Yes	Yes	No	No	0	01C0	0000	01D0
1 & 17	No	No	No	0	No	Yes	No	No	0	01C1	7984	79C5
2 & 18	No	No	No	0	Yes	Yes	No	No	0	01C2	01E0	01E2
3 & 19	No	No	No	0	Yes	Yes	No	No	0	01C3	01E0	01E3
4 & 20	No	No	No	0	Yes	Yes	Yes	No	0	01C4	01E0	01E4
5 & 21	No	No	No	0	Yes	Yes	Yes	No	0	01C5	01E0	01E5
6 & 22	No	No	No	0	No	Yes	Yes	No	0	01C6	01E0	01E6
7 & 23	No	No	No	0	No	Yes	Yes	No	0	01C7	01E0	01E7
8 & 24	No	No	No	0	No	Yes	Yes	No	0	01C8	01E0	01E8
9 & 25	No	No	Yes	0	No	Yes	Yes	No	0	01C9	01E0	01E9
10 & 26	No	No	Yes	0	No	Yes	Yes	No	0	01CA	01E0	01EA
11 & 27	No	No	Yes	0	No	Yes	Yes	No	0	01CB	01E0	01EB
12 & 28	No	No	Yes	0	No	Yes	Yes	No	0	01CC	01E0	01EC
13 & 29	No	No	Yes	0	No	Yes	Yes	No	0	01CD	01E0	01ED
14 & 30	No	No	Yes	0	No	Yes	Yes	No	0	01CE	01E0	01EE
15 & 31	No	No	Yes	0	No	Yes	Yes	No	0	01CF	01E0	01EF

BIU Mode Code Descriptor Table 2												
Mode Code	Control Word									Status List Pointer	Data List Pointer	Unused
	Interrupt On Receipt (w/o)	Illegalize Broadcast (w/o)	Illegalize Mode Code (w/o)	Reserved	Illegalize Broadcast (with data)	Illegalize Transmit (with data)	Illegalize Receive (with data)	Interrupt On Receipt	Index			
0 & 16	No	No	Yes	0	Yes	Yes	No	No	0	01C0	0000	01D0
1 & 17	No	No	No	0	No	Yes	No	No	0	01C1	7984	79C5
2 & 18	No	No	No	0	Yes	Yes	No	No	0	01C2	01E0	01E2
3 & 19	No	No	No	0	Yes	Yes	No	No	0	01C3	01E0	01E3

BIU Mode Code Descriptor Table 2												
Mode Code	Control Word									Status List Pointer	Data List Pointer	Unused
	Interrupt On Receipt (w/o)	Illegalize Broadcast (w/o)	Illegalize Mode Code (w/o)	Reserved	Illegalize Broadcast (with data)	Illegalize Transmit (with data)	Illegalize Receive (with data)	Interrupt On Receipt	Index			
4 & 20	No	No	No	0	Yes	Yes	Yes	No	0	01C4	01E0	01E4
5 & 21	No	No	No	0	Yes	Yes	Yes	No	0	01C5	01E0	01E5
6 & 22	No	No	No	0	No	Yes	Yes	No	0	01C6	01E0	01E6
7 & 23	No	No	No	0	No	Yes	Yes	No	0	01C7	01E0	01E7
8 & 24	No	No	No	0	No	Yes	Yes	No	0	01C8	01E0	01E8
9 & 25	No	No	Yes	0	No	Yes	Yes	No	0	01C9	01E0	01E9
10 & 26	No	No	Yes	0	No	Yes	Yes	No	0	01CA	01E0	01EA
11 & 27	No	No	Yes	0	No	Yes	Yes	No	0	01CB	01E0	01EB
12 & 28	No	No	Yes	0	No	Yes	Yes	No	0	01CC	01E0	01EC
13 & 29	No	No	Yes	0	No	Yes	Yes	No	0	01CD	01E0	01ED
14 & 30	No	No	Yes	0	No	Yes	Yes	No	0	01CE	01E0	01EE
15 & 31	No	No	Yes	0	No	Yes	Yes	No	0	01CF	01E0	01EF

APPENDIX I: CAPS Maintenance Housekeeping Stream Format

APPENDIX J: CAPS Maintenance Housekeeping Stream Parameter Limits

APPENDIX K: CAPS Science Housekeeping Stream Format

APPENDIX L: CAPS Science Housekeeping Stream Parameter Limits

APPENDIX M: Actuator Data Tables

Acceleration/Deceleration Table

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78, 32, 25, 21, 19, 16, 16, 14, 14, 12, 12, 12, 11, 11, 10, 10, 10, 9, 9, 9, 9, 8,
 8, 8, 8, 8, 8, 7, 8, 7, 7, 7, 7, 7, 6, 7, 6, 7, 6, 6, 6, 6, 6, 6,
 6, 6, 6, 6, 5, 6, 5, 6, 5, 5, 6, 5, 5, 5, 6, 5, 5, 5, 5, 5, 4, 5,
 5, 5, 5, 4, 5, 5, 4, 5, 4, 5, 4, 5, 4, 5, 4, 4, 5, 4, 4, 4, 5, 4,
 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 3, 4, 4, 4,
 3, 4, 4, 3, 4, 4, 3, 4, 4, 3, 4, 3, 4, 3, 4, 3, 4, 3, 4, 3, 4, 3,
 3, 4, 3, 4, 3, 3, 4, 3, 3, 4, 3, 3, 3, 4, 3, 3, 3, 3, 4, 3, 3, 3,
 3, 4, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,
 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 2, 3, 3, 3, 3, 3, 2, 3, 3, 3, 3, 2,
 3, 3, 3, 3, 2, 3, 3, 3, 2, 3, 3, 2, 3, 3, 2, 3, 3, 2, 3, 3, 2, 3,
 3, 2, 3, 3, 2, 3, 2, 3, 3, 2, 3, 2, 3, 3, 2, 3, 2, 3, 2, 3, 2, 3,
 2, 3, 2, 3, 2, 3, 2, 3, 2, 3, 2, 3, 2, 3, 2, 3, 2, 2, 3, 2, 3, 2,
 2, 3, 2, 3, 2, 2, 3, 2, 3, 2, 2, 3, 2, 2, 3, 2, 2, 3, 2, 2, 3, 2,
 2, 3, 2, 2, 3, 2, 2, 2, 3, 2, 2, 3, 2, 2, 2, 3, 2, 2, 2, 3, 2, 2,
 2, 3, 2, 2, 2, 2, 3, 2, 2, 2, 3, 2, 2, 2, 2, 3, 2, 2, 2, 2, 2, 2,
 3, 2, 2, 2, 2, 2, 2, 3, 2, 2, 2, 2, 2, 2, 2, 3, 2, 2, 2, 2, 2, 2,
 2, 2, 2, 2, 3, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 1, 2, 2, 2, 2, 2, 2,
 2, 2, 2, 2, 2, 2, 1, 2, 2, 2, 2, 2, 2, 2, 2, 1, 2, 2, 2, 2, 2, 2,
 2, 1, 2, 2, 2, 2, 2, 2, 1, 2, 2, 2, 2, 2, 1, 2, 2, 2, 2, 2, 1, 2,
 2, 2, 2, 2, 1, 2, 2, 2, 2, 1, 2, 2, 2, 2, 1, 2, 2, 2, 2, 1, 2, 2,
 2, 1, 2, 2, 2, 2, 1, 2, 2, 2, 1, 2, 2, 2, 1, 2, 2, 2, 1, 2, 2, 2,
 1, 2, 2, 2, 1, 2, 2, 2, 1, 2, 2, 1, 2, 2, 2, 1, 2, 2, 1, 2, 2, 2,
 1, 2, 2, 1, 2, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2,
 1, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2, 1, 2, 2, 1,
 2, 1, 2, 2, 1, 2, 2, 1, 2, 1, 2, 2, 1, 2, 2, 1, 2, 1, 2, 2, 1, 2,
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 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1,
 1, 1, 2, 1, 2, 1, 1, 2, 1, 2, 1, 1, 2, 1, 2, 1, 1, 2, 1, 2, 1, 1,
 2, 1, 2, 1, 1, 2, 1, 2, 1, 1, 2, 1, 1, 2, 1, 2, 1, 1, 2, 1, 1, 2,
 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1,
 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2,
 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 1, 2, 1, 1, 2, 1, 1, 2,
 1, 1, 2, 1, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 1, 2, 1, 1, 2, 1, 1,
 1, 2, 1, 1, 2, 1, 1, 1, 2, 1, 1, 2, 1, 1, 1, 2, 1, 1, 2, 1, 1, 1,
 2, 1, 1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1,
 1, 2, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1,
 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 2,
 1, 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1, 1, 1, 2, 1,
 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 1,
 1, 2, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 2, 1, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 2, 1,
 1, 1, 1, 2, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1,
 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1,
 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1,
 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1,
 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1,
 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1,
 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1,
 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1,
 1, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1,
 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1, 1,
 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 1,
 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
 1, 1, 1, 1, 1, 1, 2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1
```

EM Actuator Data

Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B
1	127	136	2	126	136	3	125	136	4	123	136	5	122	136	6	120	136	7	119	136	8	117	136
9	116	136	10	114	136	11	113	137	12	111	137	13	110	137	14	108	137	15	107	138	16	106	138
17	104	138	18	103	138	19	101	139	20	100	139	21	98	139	22	97	140	23	95	140	24	94	141
25	93	141	26	91	142	27	90	142	28	88	143	29	87	143	30	86	144	31	84	144	32	83	145
33	82	145	34	80	146	35	79	146	36	78	147	37	76	148	38	75	148	39	74	149	40	72	150
41	71	150	42	70	151	43	68	152	44	67	153	45	66	153	46	65	154	47	63	155	48	62	156
49	61	157	50	60	157	51	58	158	52	57	159	53	56	160	54	55	161	55	54	162	56	53	163
57	51	164	58	50	165	59	49	166	60	48	167	61	47	168	62	46	169	63	45	170	64	44	171
65	43	172	66	42	173	67	41	174	68	40	175	69	39	176	70	38	177	71	37	178	72	36	179
73	35	181	74	34	182	75	33	183	76	32	184	77	31	185	78	30	186	79	29	188	80	29	189
81	28	190	82	27	191	83	26	193	84	25	194	85	25	195	86	24	196	87	23	198	88	22	199
89	22	200	90	21	91	91	20	203	92	20	204	93	19	206	94	18	207	95	18	208	96	17	210
97	17	211	98	16	212	99	16	214	100	15	215	101	15	216	102	14	218	103	14	219	104	13	221
105	13	222	106	12	223	107	12	225	108	11	226	109	11	228	110	11	229	111	10	231	112	10	232
113	10	234	114	10	235	115	9	236	116	9	238	117	9	239	118	9	241	119	8	242	120	8	244
121	8	245	122	8	247	123	8	248	124	8	250	125	8	251	126	8	253	127	8	255	128	8	127
129	8	126	130	8	125	131	8	123	132	8	122	133	8	120	134	8	119	135	8	117	136	8	116
137	8	114	138	8	113	139	8	111	140	9	110	141	9	108	142	9	107	143	9	106	144	10	104
145	10	103	146	10	101	147	10	100	148	11	98	149	11	97	150	11	95	151	12	94	152	12	93
153	13	91	154	13	90	155	14	88	156	14	87	157	15	86	158	15	84	159	16	83	160	16	82
161	17	80	162	17	79	163	18	78	164	18	76	165	19	75	166	20	74	167	20	72	168	21	71
169	22	70	170	22	68	171	23	67	172	24	66	173	25	65	174	25	63	175	26	62	176	27	61
177	28	60	178	29	58	179	29	57	180	30	56	181	31	55	182	32	54	183	33	53	184	34	51
185	35	50	186	36	49	187	37	48	188	38	47	189	39	46	190	40	45	191	41	44	192	42	43
193	43	42	194	44	41	195	45	40	196	46	39	197	47	38	198	48	37	199	49	36	200	50	35
201	51	34	202	53	33	203	54	32	204	55	31	205	56	30	206	57	29	207	58	29	208	60	28
209	61	27	210	62	26	211	63	25	212	65	25	213	66	24	214	67	23	215	68	22	216	70	22
217	71	21	218	72	20	219	74	20	220	75	19	221	76	18	222	78	18	223	79	17	224	80	17
225	82	16	226	83	16	227	84	15	228	86	15	229	87	14	230	88	14	231	90	13	232	91	13
233	93	12	234	94	12	235	95	11	236	97	11	237	98	11	238	100	10	239	101	10	240	103	10
241	104	10	242	106	9	243	107	9	244	108	9	245	110	9	246	111	8	247	113	8	248	114	8
249	116	8	250	117	8	251	119	8	252	120	8	253	122	8	254	123	8	255	125	8	256	127	8
257	255	8	258	254	8	259	253	8	260	251	8	261	250	8	262	248	8	263	247	8	264	245	8
265	244	8	266	242	8	267	241	9	268	239	9	269	238	9	270	236	9	271	235	10	272	234	10
273	232	10	274	231	10	275	229	11	276	228	11	277	226	11	278	225	12	279	223	12	280	222	13
281	221	13	282	219	14	283	218	14	284	216	15	285	215	15	286	214	16	287	212	16	288	211	17
289	210	17	290	208	18	291	207	18	292	206	19	293	204	20	294	203	20	295	202	21	296	200	22
297	199	22	298	198	23	299	196	24	300	195	25	301	194	25	302	193	26	303	191	27	304	190	28
305	189	29	306	188	29	307	186	30	308	185	31	309	184	32	310	183	33	311	182	34	312	181	35
313	179	36	314	178	37	315	177	38	316	176	39	317	175	40	318	174	41	319	173	42	320	172	43
321	171	44	322	170	45	323	169	46	324	168	47	325	167	48	326	166	49	327	165	50	328	164	51

Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B
329	163	53	330	162	54	331	161	55	332	160	56	333	159	57	334	158	58	335	157	60	336	157	61
337	156	62	338	155	63	339	154	65	340	153	66	341	153	67	342	152	68	343	151	70	344	150	71
345	150	72	346	149	75	347	148	75	348	148	76	349	147	78	350	146	79	351	146	80	352	145	82
353	145	83	354	144	84	355	144	86	356	143	87	357	143	88	358	142	90	359	142	91	360	141	93
361	141	94	362	140	95	363	140	97	364	139	98	365	139	100	366	139	101	367	138	103	368	138	104
369	138	106	370	138	107	371	137	108	372	137	110	373	137	111	374	137	113	375	136	114	376	136	116
377	136	117	378	136	119	379	136	120	380	136	122	381	136	123	382	136	125	383	136	127	384	136	255
385	136	254	386	136	253	387	136	251	388	136	250	389	136	248	390	136	247	391	136	245	392	136	244
393	136	242	394	136	241	395	136	239	396	137	238	397	137	236	398	137	235	399	137	234	400	138	232
401	138	231	402	138	229	403	138	228	404	139	226	405	139	225	406	139	223	407	140	222	408	140	221
409	141	219	410	141	218	411	142	216	412	142	215	413	143	214	414	143	212	415	144	211	416	144	210
417	145	208	418	145	207	419	146	206	420	146	204	421	147	203	422	148	202	423	148	200	424	149	199
425	150	198	426	150	196	427	151	195	428	152	194	429	153	193	430	153	191	431	154	190	432	155	189
433	156	188	434	157	186	435	157	185	436	158	184	437	159	183	438	160	182	439	161	181	440	162	179
441	163	178	442	164	177	443	165	176	444	166	175	445	167	174	446	168	173	447	169	172	448	170	171
449	171	170	450	172	169	451	173	168	452	174	167	453	175	166	454	176	165	455	177	164	456	178	163
457	179	162	458	181	161	459	182	160	460	183	159	461	184	158	462	185	157	463	186	157	464	188	156
465	189	155	466	190	154	467	191	153	468	193	153	469	194	152	470	195	151	471	196	150	472	198	150
473	199	149	474	200	148	475	202	148	476	203	147	477	204	146	478	206	146	479	207	145	480	208	145
481	210	144	482	211	144	483	212	143	484	214	143	485	215	142	486	216	142	487	218	141	488	219	141
489	221	140	490	222	140	*491	223	139	492	225	139	493	226	139	494	228	138	495	229	138	496	231	138
497	232	138	498	234	137	499	235	137	500	236	137	501	238	137	502	239	136	503	241	136	504	242	136
505	244	136	506	245	136	507	247	136	508	248	136	509	250	136	510	251	136	511	253	136	512	255	136

FM Actuator Data

Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B
1	254	3	2	252	3	3	250	3	4	248	4	5	245	4	6	243	4	7	241	4	8	238	4
9	236	4	10	234	5	11	231	5	12	229	5	13	227	5	14	225	6	15	223	6	16	220	7
17	218	7	18	216	7	19	214	8	20	212	8	21	210	9	22	208	10	23	207	10	24	205	11
25	203	11	26	201	12	27	200	13	28	198	13	29	196	14	30	195	15	31	193	15	32	192	16
33	190	17	34	189	18	35	188	18	36	186	19	37	185	20	38	184	20	39	183	21	40	181	22
41	180	23	42	179	23	43	178	24	44	177	25	45	176	26	46	175	26	47	174	27	48	173	28
49	172	28	50	171	29	51	170	30	52	170	31	53	169	31	54	168	32	55	167	33	56	166	33
57	166	34	58	165	35	59	164	35	60	164	36	61	163	37	62	162	38	63	162	38	64	161	39
65	160	40	66	160	40	67	159	41	68	158	42	69	158	42	70	157	43	71	157	44	72	156	45
73	156	45	74	155	46	75	154	47	76	154	47	77	153	48	78	153	49	79	152	50	80	152	51
81	151	52	82	150	52	83	150	53	84	149	54	85	149	55	86	148	56	87	148	57	88	147	58
89	147	59	90	146	60	91	145	61	92	145	62	93	144	63	94	144	64	95	143	66	96	143	67
97	142	68	98	141	69	99	141	71	100	140	72	101	140	74	102	139	75	103	139	76	104	138	78
105	138	80	106	137	81	107	137	83	108	136	85	109	136	86	110	135	88	111	135	90	112	135	92
113	134	94	114	134	96	115	133	98	116	133	100	117	133	102	118	133	104	119	132	106	120	132	108
121	132	111	122	132	113	123	132	115	124	131	118	125	131	120	126	131	122	127	131	124	128	131	125
129	131	253	130	131	252	131	131	250	132	131	248	133	131	246	134	132	244	135	132	241	136	132	239
137	132	236	138	132	234	139	133	232	140	133	229	141	133	227	142	134	225	143	134	223	144	134	221
145	135	219	146	135	217	147	136	215	148	136	213	149	137	211	150	137	209	151	138	207	152	139	205
153	139	203	154	140	202	155	140	200	156	141	198	157	142	197	158	142	195	159	143	194	160	144	192
161	145	191	162	145	189	163	146	188	164	147	187	165	147	185	166	148	184	167	149	183	168	150	182
169	150	181	170	151	179	171	152	178	172	153	177	173	153	176	174	154	175	175	155	174	176	155	173
177	156	172	178	157	172	179	158	171	180	158	170	181	159	169	182	160	168	183	160	167	184	161	167
185	162	166	186	163	165	187	163	165	188	164	164	189	165	163	190	165	162	191	166	162	192	167	161
193	167	161	194	168	160	195	169	159	196	169	159	197	170	158	198	171	158	199	172	157	200	172	156
201	173	156	202	174	155	203	174	155	204	175	154	205	176	154	206	177	153	207	178	152	208	178	152
209	179	151	210	180	151	211	181	150	212	182	150	213	183	149	214	184	148	215	185	148	216	186	147
217	187	147	218	188	146	219	189	146	220	190	145	221	191	145	222	192	144	223	193	143	224	195	143
225	196	142	226	197	142	227	198	141	228	200	141	229	201	140	230	203	140	231	204	139	232	206	138
233	207	138	234	209	137	235	211	137	236	212	137	237	214	136	238	216	136	239	218	135	240	220	135
241	221	134	242	223	134	243	226	134	244	228	133	245	230	133	246	232	133	247	234	133	248	236	132
249	238	132	250	240	132	251	243	132	252	245	132	253	247	132	254	250	131	255	252	131	256	254	131
257	126	131	258	124	131	259	122	131	260	120	132	261	117	132	262	115	132	263	113	132	264	110	132
265	108	132	266	106	133	267	103	133	268	101	133	269	99	133	270	97	134	271	95	134	272	92	135
273	90	135	274	88	135	275	86	136	276	84	136	277	82	137	278	80	138	279	79	138	280	77	139
281	75	139	282	73	140	283	72	141	284	70	141	285	68	142	286	67	143	287	65	143	288	64	144
289	62	145	290	61	146	291	60	146	292	58	147	293	57	148	294	56	148	295	55	149	296	53	150
297	52	151	298	51	151	299	50	152	300	49	153	301	48	154	302	47	154	303	46	155	304	45	156
305	44	156	306	43	157	307	42	158	308	42	159	309	41	159	310	40	160	311	39	161	312	38	161
313	38	162	314	37	163	315	36	163	316	36	164	317	35	165	318	34	166	319	34	166	320	33	167

Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B	Step	A	B
321	32	168	322	32	168	323	31	169	324	30	170	325	30	170	326	29	171	327	29	172	328	28	173
329	28	173	330	27	174	331	26	175	332	26	175	333	25	176	334	25	177	335	24	178	336	24	179
337	23	180	338	22	180	339	22	181	340	21	182	341	21	183	342	20	184	343	20	185	344	19	186
345	19	187	346	18	188	347	17	189	348	17	190	349	16	191	350	16	192	351	15	194	352	15	195
353	14	196	354	13	197	355	13	199	356	12	200	357	12	202	358	11	203	359	11	204	360	10	206
361	10	208	362	9	209	363	9	211	364	8	213	365	8	214	366	7	216	367	7	218	368	7	220
369	6	222	370	6	224	371	5	226	372	5	228	373	5	230	374	5	232	375	4	234	376	4	236
377	4	239	378	4	241	379	4	243	380	3	246	381	3	248	382	3	250	383	3	252	384	3	253
385	3	125	386	3	124	387	3	122	388	3	120	389	3	118	390	4	116	391	4	113	392	4	111
393	4	108	394	4	106	395	5	104	396	5	101	397	5	99	398	6	97	399	6	95	400	6	93
401	7	91	402	7	89	403	8	87	404	8	85	405	9	83	406	9	81	407	10	79	408	11	77
409	11	75	410	12	74	411	12	72	412	13	70	413	14	69	414	14	67	415	15	66	416	16	64
417	17	63	418	17	61	419	18	60	420	19	59	421	19	57	422	20	56	423	21	55	424	22	54
425	22	53	426	23	51	427	24	50	428	25	49	429	25	48	430	26	47	431	27	46	432	27	45
433	28	44	434	29	44	435	30	43	436	30	42	437	31	41	438	32	40	439	32	39	440	33	39
441	34	38	442	35	37	443	35	37	444	36	36	445	37	35	446	37	34	447	38	34	448	39	33
449	39	33	450	40	32	451	41	31	452	41	31	453	42	30	454	43	30	455	44	29	456	44	28
457	45	28	458	46	27	459	46	27	460	47	26	461	48	26	462	49	25	463	50	24	464	50	24
465	51	23	466	52	23	467	53	22	468	54	22	469	55	21	470	56	20	471	57	20	472	58	19
473	59	19	474	60	18	475	61	18	476	62	17	477	63	17	478	64	16	479	65	15	480	67	15
481	68	14	482	69	14	483	70	13	484	72	13	485	73	12	486	75	12	487	76	11	488	78	10
489	79	10	490	81	9	491	83	9	492	84	9	493	86	8	494	88	8	495	90	7	496	92	7
497	93	6	498	95	6	499	98	6	500	100	5	501	102	5	502	104	5	503	106	5	504	108	4
505	110	4	506	112	4	507	115	4	508	117	4	509	119	4	510	122	3	511	124	3	512	126	3

APPENDIX N: Command Summary and Formats

This appendix contains a command summary list of all CAPS commands. The command summary column headed “W” indicates the CAPS commands MUST be wrapped before being submitted to JPL’s ground system (SEQTRAN). The column headed “Type” indicates the commands used only by the PROM software, used only by the Science software. Sub-column “P” indicates the CAPS commands recognized by the CPU1 PROM software (Maintenance, CPU2/SAM_Ready and Low Voltage modes). The sub-column headed “R” indicates the CAPS commands recognized by the DPU software loaded into RAM from the ground or the SSR (CPU1/CPU2/SAM software). Within each column, the supported modes are indicated. They are as follows: L – Low Power, M – Maintenance, C – CPU2/SAM_Ready, N – Normal Science, S – Sleep. A subscript of OPW indicates the command is valid only when the OPWART power mode is active. The column titled “Boundary” indicates the CAPS boundary(ies) associated with each command. A mark in sub-column “I” indicates the command is executed immediately upon receipt by the target CPU. A mark in sub-column “A” indicates the command is executed on the A-cycle boundary followed by the receipt of an 82DPU_A_CYCLE command. A mark in sub-column “B” indicates the command is executed on the B-cycle boundary followed by the receipt of an 82DPU_B_CYCLE command. If the column is marked with an indicator other than a “·”, then the boundary condition has constraints as listed in the footnotes.

This appendix also contains command descriptions for each command. These descriptions were provided to JPL as input to the JPL documentation CAS-3-291.

CAPS COMMAND SUMMARY								
Command	W†	Type*		Boundary††			Opcode	Description
		P	R	I	A	B		
82ACT_EXEC	×	L, M	N_{opw}	·	·	·	64 (40h)	Initiates/stops ACT operations and sets ACT rate
82ACT_FOV	×	L, M	L, N, S	·	·	·	65 (41h)	Defines the ACT field of view and operational mode
82ACT_LAT_CNTRL	×	L, M		·			66 (42h)	Enables/disables ACT launch latch release
82ACT_LAT_STATE	×	L, M		·			67 (43h)	Turns the ACT launch latch state to SAFE/ARM
82ACT_LATCH		L, M		·			68 (44h)	Releases the ACT launch latch
82ACT_TEMP_COMP	×		L, N, S	·			69 (45h)	Enables/disables ACT temp. compensation algorithm
82ACT_WOBL_COMP	×		L, N, S	·			70 (46h)	Enables/disables ACT wobble compensation algorithm
82ALF		L, M, C	L, N, S	·			32 (20h)	Forward an ALF Data Block to CAPS
82ALF_END		L, M, C	L, N, S	·			35 (23h)	Forward an ALF Terminator (End) Block to CAPS
82ALF_RANGE		L, M, C	L, N, S	·			36 (24h)	Define a range of blocks to extract from ALF data load
82ALF_SKIP		L, M, C	L, N, S	·			37 (25h)	Forward an ALF Skip Block to CAPS
82ALF_XTREMES		L, M, C	L, N, S	·			38 (26h)	Define the range of ALF sequence numbers
82CPU1_MRO	×		N		·		49 (31h)	Puts CPU1 in MRO mode for 1 A-cycle
82CPU1_RAM_ADDR		L, C	L	·			50 (32h)	Supplies the beginning address for CPU1 RAM exec
82CPU1_RAM_EXEC		C	L	·			51 (33h)	Instructs CPU1 to begin executing at given RAM addr
82CPU1_WATCHDOG	×	L, M, C	L, N, S	·			52 (34h)	Enables/disables CAPS CPU1 watchdog function
82CPU2_CNTRL	×	L, M, C	Opw	·			176 (B0h)	Holds or releases CPU2 µprocessor reset
82CPU2_EVNT_MODE	×		N			·	177 (B1h)	Defines and initiates CPU2 Event mode
82CPU2_INTEGRITY	×		L, N, S	·			178 (B2h)	Commands CPU2 to perform memory integrity checks
82CPU2_MRO	×		N			·	180 (B4h)	Commands CPU2 to MRO mode (for 2 A-cycles)
82CPU2_RAM_ADDR		L, M, C	L, N, S	·			181 (B5h)	Supplies the beginning address for CPU2 RAM exec
82CPU2_RAM_EXEC		L, M, C	L, N, S	·			182 (B6h)	Instructs CPU2 to begin executing at given RAM addr
82CPU2_RESET		L, M, S	L, N, S	·			183 (B7h)	Resets and releases CPU2 (software pulse reset)
82CPU2_TOF_LEF	×		N			·	184 (B8h)	Configures how TOF LEF data product is produced
82CPU2_TOF_ST	×		N			·	185 (B9h)	Configures how TOF ST data product is produced
82CPU2_WATCHDOG	×		N	·			186 (BAh)	Enables/disables CAPS CPU2 watchdog function
82DPU_A_CYCLE	×	L, M, C	L, N, S	·			160 (A0h)	Signals DPU to execute all queued A-cycle commands
82DPU_B_CYCLE	×		N	·			161 (A1h)	Signals DPU to execute all queued B-cycle commands

CAPS COMMAND SUMMARY								
Command	W[†]	Type*		Boundary[††]			Opcode	Description
82DPU_ACQ	×		L,N,S		·	·	171 (ABh)	DPU acquisition and compression strategies
82DPU_BACKGND	×		N			·	162 (A2h)	Enables/disables background measurements
82DPU_BIU_INTGRTY			N		·	·	174 (AEh)	Instructs DPU to perform BIU integrity tests
82DPU_BKGND_INT	×		N			·	163 (A3h)	Defines the interval for background measurements
82DPU_CLEAR_ERRS	×	L, M, C	L, N, S	·			164 (A4h)	Clears (zeros) all error indicators in the DPU
82DPU_HK_FORMAT	×	L, M, C			·		165 (A5h)	Specifies telemetry housekeeping format
82DPU_HK_MRO	×	L, M, C	L, N, S		·		166 (A6h)	Defines contents of the housekeeping MRO words
82DPU_MODE		L, M, C	L, N, S	·	·	·	167 (A7h)	Instructs DPU to enter a predefined operating mode
82DPU_SCLK_MULTR	×		N	·	·	·	175 (AFh)	Specifies the CAPS Sample Clock multiplier
82DPU_SUPHTR_PWR		L, M, C	L, N, S	·			170 (AAh)	Turns CAPS Supplemental Heater power ON/OFF
82DPU_TLM_RATE	×		N		·	·	172 (ACh)	Specifies CAPS logical telemetry rate
82DPU_TRAFFIC	×		N		·	·	173 (ADh)	Enables/disables DPU telemetry output by sensor
82ELS_DTM_CNTRL	×		N		·		80 (50h)	Enables/disables ELS dead time correction alg
82ELS_DTM_PERIOD	×		N		·		91 (5Bh)	selects ELS dead time to be 1/8 or 1/4 of the sample period
82ELS_GRID_CNTRL	×		N		·		92 (5Ch)	Enables/disables ELS Grid function
82ELS_HV_PWR			N	·			93 (5Dh)	Turns the ELS +15V supply for HV ON/OFF
82ELS_MCP_ADJ	×		N	·	·		82 (52h)	Specifies the ELS MCP HV power supply level
82ELS_MCP_PWR			N	·			83 (53h)	Turns power to the ELS MCP HV supply ON/OFF
82ELS_STIM	×		N	·	·		84 (54h)	Defines ELS STIM amplitude, mode, and state
82ELS_SUM_AVG	×		L, N, S		·		94 (5Eh)	Set the ELS data product summing or averaging
82ELS_SWP_PWR			N	·			81 (51h)	Turns power to the ELS HV Sweep supply ON/OFF
82ELS_MODE_A	×		N		·		85 (55h)	Configures and enters ELS sweep supply Mode A
82ELS_MODE_B	×		N		·		86 (56h)	Configures and enters ELS sweep supply Mode B
82ELS_MODE_C0	×		N		·		87 (57h)	Configures and enters ELS sweep supply Mode C0
82ELS_MODE_C1	×		N		·		88 (58h)	Configures and enters ELS sweep supply Mode C1
82ELS_MODE_D	×		N		·		89 (59h)	Configures and enters ELS sweep supply Mode D
82ELS_MODE_E	×		N		·		90 (5Ah)	Configures and enters ELS sweep supply Mode E
82ELS_THRESHOLD	×		N	·	·	·	150 (96h)	Specifies count sensitivity thresholds for the ELS sensor

CAPS COMMAND SUMMARY								
Command	W†	Type*		Boundary††			Opcode	Description
82FEE_BIT_CNTRL	×		N	·	·	·	208 (D0h)	Defines the FEE configuration reg BIT control fields
82FEE_BIT_CONFIG	×		N	·	·	·	209 (D1h)	Specifies FEE BIT configuration regs #1 and #2 values
82FEE_STARTS	×		N	·	·	·	210 (D2h)	Defines the FEE config. reg Starts, MedRes, and HiRes Stop fields
82FEE_THRESH	×		N			·	211 (D3h)	Defines the TDC and FEE config regs' Threshold fields
82HVU1_ACC_ADJ	×		N	·	·	·	144 (90h)	Specifies the Accelerating HV supply level
82HVU1_CNTRL	×		N	·			145 (91h)	Enables/disables the HVU1 supply
82HVU1_PWR1			N	·			146 (92h)	Turns power switch #1 to the HVU1 ON/OFF
82HVU1_PWR2			N	·			147 (93h)	Turns power switch #2 to the HVU1 ON/OFF
82HVU1_RET_ADJ	×		N	·	·	·	148 (94h)	Specifies the Retarding HV supply level
82HVU1_STATE	×		N	·			149 (95h)	Turns HVU1 operating state SAFE/ARM
82HVU2_CNTRL	×		N	·			152 (98h)	Enables/disables the HVU2 supply
82HVU2_ESA_ADJ	×		N	·	·	·	153 (99h)	Specifies the ESA HV supply level
82HVU2_LEF_ADJ	×		N	·	·	·	154 (9Ah)	Specifies the LEF HV supply level
82HVU2_PWR			N	·			155 (9Bh)	Turns power to the HVU2 ON/OFF
82HVU2_ST_ADJ	×		N	·	·	·	156 (9Ch)	Specifies the Straight-Through HV level
82HVU2_STATE	×		N	·			157 (9Dh)	Turns HVU2 operating state SAFE/ARM
82HVU2_SWP_CNTRL	×		N	·	·	·	158 (9Eh)	Enables/disables HVU2 ESA sweeping
82IBS_CEM_ADJ	×		N	·	·		104 (68h)	Specifies IBS CEM HV supply level
82IBS_DTM_CNTRL	×		N		·		105 (69h)	Enables/disables IBS dead time correction algorithm
82IBS_ESA_ADJ	×		N	·	·		106 (6Ah)	Specifies IBS ESA HV supply level
82IBS_HV_CNTRL	×		N	·			107 (6Bh)	Enables/disables the IBS HV supply
82IBS_HV_PWR			N	·			108 (6Ch)	Turns power to the IBS HV supply ON/OFF
82IBS_HV_STATE	×		N	·			109 (6Dh)	Turns IBS HV supply operating state SAFE/ARM
82IBS_MODE	×		L, N, S		·	·	111 (6Fh)	Selects IBS data acquisition mode
82IBS_STIM	×		N	·	·		110 (6Eh)	Specifies IBS STIM channels, frequency, and state
82IBS_STIM_TBL	×		N	·	·		101 (65h)	Selects IBS STIM Table
82IBS_SWP_CNTRL	×		N	·	·		103 (67h)	Enables/disables IBS ESA sweeping
82IBS_THRESHOLD	×		N	·	·	·	99 (63h)	Specifies count sensitivity thresholds for the IBS sensor

CAPS COMMAND SUMMARY								
Command	W†	Type*		Boundary††			Opcode	Description
82IMS_COV_CNTRL	×	L, M		·			112 (70h)	Enables/disables IMS cover release function
82IMS_COV_STATE	×	L, M		·			113 (71h)	Turns the IMS cover release state to SAFE/ARM
82IMS_COVER		L, M		·			114 (72h)	Releases the IMS cover
82IMS_ION_CFG	×		N		·	·	118 (76h)	Selects the IMS ion configuration
82IMS_LOG_SLCT	×		N		·	·	117 (75h)	Selects the IMS logical configuration
82IMS_SWP_TBL	×		N		·	·	115 (73h)	Selects IMS Sweep Table
82IMS_THRESHOLD	×		N	·	·	·	116 (74h)	Specifies count sensitivity thresholds for the IMS sensor
82MEM_BLOCK_C			L, N, S	·			224 (E0h)	Loads critical data into DPU memory
82MEM_BLOCK_NC			L, N, S	·			225 (E1h)	Loads non-critical data into DPU memory
82MEM_LOAD_C			L, N, S	·			226 (E2h)	Defines subsequent critical data load
82MEM_LOAD_NC			L, N, S	·			227 (E3h)	Defines subsequent non-critical data load
82MEM_PATCH_C			L, N, S	·			228 (E4h)	Patches critical DPU memory/parameters
82MEM_PATCH_NC			L, N, S	·			229 (E5h)	Patches non-critical DPU memory/parameters
82NO_OP	×	L, M, S	L, N, S	·			48 (30h)	“No operation” command
82PS_CAPS				·			n/a	Turns CAPS electronics ON/OFF
82PS_HTR				·			n/a	Turns CAPS Replacement Heater ON/OFF
82RT_ARADDR				·			n/a	Selects alt RAM address as target for CAPS boot code
82RT_BIU_BIT5				·			n/a	Sets/resets the BIU Discrete Command bit #5
82RT_BIU_BIT6				·			n/a	Sets/resets the BIU Discrete Command bit #6
82RT_BIU_BIT7				·			n/a	Sets/resets the BIU Discrete Command bit #7
82RT_OPMODE				·			n/a	Specifies CAPS power interlock BIU discrete cmd bits
82RT_RESET				·			n/a	Specifies CAPS subsystem reset BIU discrete cmd bit
82RT_WDTERR_CAPS				·			n/a	Enables/disables BIU Watchdog Timer Expired Flag
82RT_WPERR_CAPS				·			n/a	Clears/sets BIU Write Protection Violation Flag
82RT_WPFNC_CAPS				·			n/a	Enables/disables BIU Write Protect Function
82RT_WTA_ILOCK				·			n/a	Sets/resets the WTA interlock BIU discrete cmd bit
82SAM_BKGD_CNTRL	×		N		·	·	192 (C0h)	Enables/disables SAM background compensation
82SAM_CNFG_IDX	×		N			·	202 (CAh)	Selects SAM 1750A Configuration 1 or 2
82SAM_DTM_CNTRL	×		N			·	193 (C1h)	Enables/disables the SAM dead time correction

CAPS COMMAND SUMMARY								
Command	W[†]	Type*		Boundary[††]			Opcode	Description
82SAM_DTM_CONST	×		N			·	194 (C2h)	Specifies the SAM dead time correction constant
82SAM_FAULT_CNTRL	×		N			·	204 (CCh)	Enables/disables SAM Fault Modes
82SAM_GROUP_TBL	×		N			·	195 (C3h)	Selects SAM Group Table
82SAM_HBLUT_INDX	×		N			·	196 (C4h)	Specifies The SAM Hardware Binning Look Up Table
82SAM_ION_SELECT	×		N		·	·	198 (C6h)	Defines SAM ION Output Selection Index
82SAM_MLUT_INDX	×		N			·	199 (C7h)	Selects SAM Molecule Look Up Table Index
82SAM_MOL_LEF	×		N		·	·	200 (C8h)	Selects SAM Molecule and/or LEF data products
82SAM_SECTOR	×		N			·	205 (CDh)	Enables/disables CAPS SAM Anode Sectors
82SEQ_BLOCK			L, N, S	·			1 (01h)	Loads distributed sequence data into DPU memory
82SEQ_CHECKSUM		L, M, C	L, N, S	·			2 (02h)	Calculates and tests distributed sequence checksum
82SEQ_END		L, M, C	L, N, S	·			3 (03h)	Ends a specific active distributive sequence
82SEQ_END_ALL		L, M, C	L, N, S	·			4 (04h)	Ends all active distributed sequences
82SEQ_LINK			L, N, S	·			5 (05h)	Links a distributed sequence to another sequence
82SEQ_LOAD			L, N, S	·			6 (06h)	Defines subsequent distributed sequence load
82SEQ_TWEAK		L, M, C	L, N, S	·			7 (07h)	Tweaks (patches) a distributed sequence
82TDC_DTM	×		N			·	215 (D7h)	Defines TDC config reg #1 Dead Time Correction
82TDC_DTM_ADJ	×		N			·	216 (D8h)	Selects TDC config reg #2 Dead Time Correction Adjust
82TDC_ENG_SING	×		N		·	·	217 (D9h)	Defines TDC config reg #1 Engineering Singles fields
82TDC_HITS	×		N			·	218 (DAh)	Defines the TDC config reg #1 Number of Hits fields
82TDC_ID_COIN	×		N			·	219 (DBh)	Defines the TDC config reg #1 Coincidence bits
82TDC_LOGICAL	×		N		·	·	214 (D6h)	Selects Engineering Logical 13 or 14
82TDC_MAX_TOF	×		N			·	220 (DCh)	Defines the TDC config reg #2 Max TOF value field
82TDC_RESET	×		N	·	·	·	221(DDh)	Defines the TDC config reg #1 Reset field
82TDC_STIM	×		N	·	·	·	222 (DEh)	Defines the TDC config reg #1 BIT field (BIT ON/OFF)
82TDC_VERN	×		N			·	223 (DFh)	Defines the TDC config reg #1 Vernier Adjust field
82TRIGGER		L, M, C	L, N, S	·			128 (80h)	Triggers the execution of a CAPS internal distributed sequence
82WRAP							n/a	Wraps individual internal CAPS command for inclusion in SASF